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DOE NASA CONTRACTOR REPORT

DOE NASA CR-150606

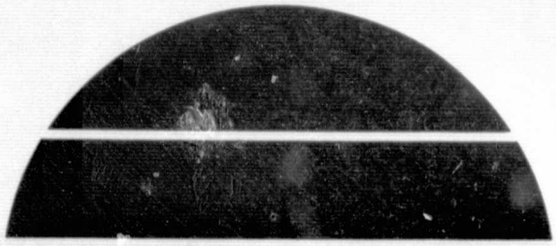
SYSTEM DESIGN PACKAGE FOR SOLAR HEATING AND COOLING SITE DATA ACQUISITION SUBSYSTEM - MOD 1

IBM Corporation
Federal Systems Division
150 Sparkman Drive
Huntsville, Alabama 35805

Under Contract NAS8-32036 with

National Aeronautics and Space Administration
George C. Marshall Space Flight Center, Alabama 35812

For the U. S. Department of Energy



U.S. Department of Energy

Solar Energy

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16. ABSTRACT

The Site Data Acquisition Subsystem (SDAS) is designed to collect data from sensors located on residential or commercial buildings using a solar heating and/or cooling system. It takes the data obtained from sensoes located on the solar system, processes the data into suitable format, stores the data for a period of time, and provides the capability for either telephone retrieval by the Central Data Processing System (CDPS) or manual retrieval of the data for transfer to a central site. The SDAS is also designed so that it will not degrade the operation of the solar heating/cooling system which it is monitoring.

This report contains documentation necessary to evaluate the design of the SDAS; i. e., SDAS Description Document, SDAS Performance Specification, and drawing list.

Some reformatting and renumbering of pages have been done for clarity only.

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SECTION A

SITE DATA ACQUISITION SUBSYSTEM (SDAS)
DESCRIPTION

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1.0 INTRODUCTION

This document describes the design and performance of the current Site Data Acquisition Subsystem (SDAS). This document defines the requirements to be met by all configurations of the Site Data Acquisition Subsystem including critical performance, installation requirements, and the detailed configuration relative to the system which it services.

2.0 RELATED DOCUMENTS (For Information Only)

The following documentation is not a part of the procurement package but is listed herein for information purposes only. Some of these documents may be helpful to prospective bidders and will be made available, subsequently, on request.

2.1 GOVERNMENT DOCUMENTS

2.1.1 Central Data Processing System Software Performance Specification, MSFC No. DR501-46, July 28, 1976.

2.1.2 Instrumentation Installation Guidelines for National Solar Heating and Cooling Demonstration Program, MSFC No. SHC-1006, August 5,

2.2 CONTRACTOR DOCUMENTS

2.2.1 Site Data Acquisition Subsystem Microprogram Description Document for current SDAS design.

2.2.2 Manufacturing drawings for current SDAS design.

3.0 GOVERNMENT FURNISHED PROPERTY

Telephone line installation and communications interface between the SDAS and Central Data Processing System (CDPS) shall be provided by the Government for those installations requiring such facilities.

4.0 SITE DATA ACQUISITION SUBSYSTEM REQUIREMENTS

Requirements for the Site Data Acquisition Subsystem are contained in the following paragraphs.

4.1 SYSTEM OVERVIEW

The Site Data Acquisition Subsystem (SDAS) shall be designed to collect data from sensors located on residential or commercial buildings using a solar heating and/or cooling system. The SDAS shall take the data obtained from sensors located on the solar heating and/or cooling system, process the data into a suitable format, store the data for a period of time, and provide the capability for either telephone retrieval by the Central Data Processing System (CDPS) or manual retrieval of the data for transfer to the central site. The unit shall be designed so it will not degrade the operation of the solar heating/cooling system which it is monitoring.

4.2 OPERATING CHARACTERISTICS

The SDAS provides the flexibility of handling inputs from a maximum of 95 sensors as identified in Paragraph 4.5 for solar energy systems and

buildings. Individual units shall be personalized for specific site inputs. A functional block diagram of the current design SDAS is shown in Figure 4.2-1. The SDAS shall, as a minimum, perform the following functions:

- Scan the input sensors for data and multiplex and condition the input data into a digital data format.
- Buffer the data for later retrieval by the central site.
- In response to an interrogation by telephone from the CDPS, transmit the stored data to the CDPS.
- The same set of SDAS software shall be used regardless of the number of channels.

The data to be transmitted to the CDPS shall be encoded for asynchronous transmission over standard-voice-grade telephone lines. Time, synchronization and BCH (error detecting) codes shall be added to the data to aid the CDPS in error detection, formatting and processing of the data from the SDAS. BCH encoding is defined in paragraph 4.4.9.

The CDPS has a command/response interface with the SDAS to prevent unauthorized access to the SDAS. The SDAS shall provide codes to enable the CDPS to detect the end of the data being transmitted. See paragraph 4.4.12.

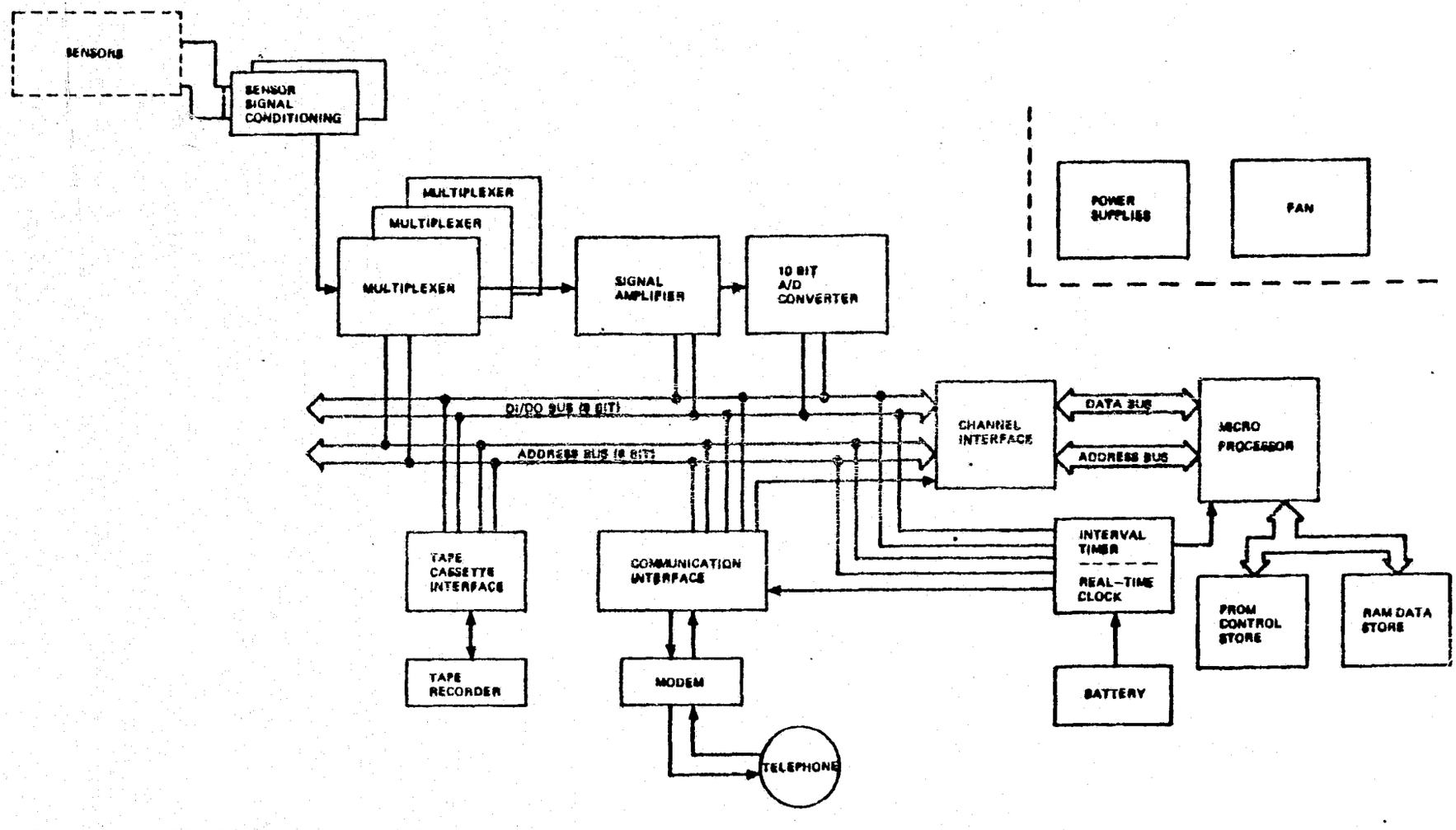

Figure 4.2-1. SDAS Functional Block Diagram

4.3 SYSTEM REQUIREMENTS

4.3.1 Time Period

The SDAS shall be designed to operate continuously for up to five years.

4.3.2 Autonomy

The SDAS shall be designed to operate unattended except for maintenance and manual collection of data.

4.3.3 Subsystem Isolation

The SDAS shall be designed such that a failure of the SDAS shall not affect the operation or performance of the installed solar heating and/or cooling system.

4.3.4 SDAS Safety

Design and installation of the SDAS shall comply with applicable electrical codes specified elsewhere in this document, and with UL certification requirements to eliminate safety hazards to the occupants of the dwelling or building during SDAS installation and operation.

4.3.5 Signal Conditioning

The SDAS shall provide the signal conditioning required on each of the 95 input channels.

4.3.6 SDAS Data Channel Modularity

The maximum number of SDAS channels needed is 96. The minimum number of SDAS channels needed for a particular application is 16. A modular approach shall be used for multiplexing and signal conditioning. The number of SDAS channels shall be incremental in groups of 16. SDAS configurations of 16, 32, 48, 64, 80 and 96 channels will be required to support the individual sites of the National Solar Heating and Cooling Program.

4.4 PERFORMANCE REQUIREMENTS

4.4.1 Data Scan Intervals

The SDAS shall have the capability of two types of scan intervals. The first type is the major scan interval. The SDAS, when in the major scan interval, shall scan all sensor input channels at N times 32 sec., where N is a manually selected value varying from 1 through 63. The second type of scan is the minor scan interval. The SDAS minor scan interval is fixed at 32 seconds. Twenty channels of the 95-channel SDAS shall be sampled at the minor scan interval and the data summed, then averaged for the duration of the major scan interval selected. The actual number of samples collected for a given major scan interval can vary due to interrupts; therefore, the average data inserted in the data stream must reflect the actual number of samples collected.

There shall be a separate manual switch that changes the basic sample time from 32 seconds to a special test scan rate of one per eight seconds.

Data from all scans shall be stored in the RAM as a record. Each record may be retrieved via telephone playback of the collected records on tape. Approximately 1.5 milliseconds is required to read one sensor channel input into the RAM.

4.4.2 A/D Resolution

The SDAS shall convert the analog inputs into 10-bit (left justified) digital words. On certain measurements, to be subsequently defined, the two LSB's may be dropped if accuracy requirements can be met with 8-bit words.

4.4.3 Calibration

A signal ground shall be included to provide an addressable channel (No. 1) for determining the accuracy of recorded data.

4.4.4 SDAS Accuracy

The SDAS shall provide a maximum error from multiplexer connector to digital word conversion of the input parameters of 0.4% $\pm$ 1/2 LSB of the full scale (5 vdc or 100 mvdc). The pluggable micro-boards to be installed in the SDAS (or other signal conditioning equipment in the SDAS) shall be included in the sensor error computations.

4.4.5 Time Tag and Coding

The SDAS shall provide a synchronization code and time tags (see paragraphs 4.4.9 and 4.4.12) to aid in central site processing. The real-time clock shall operate continuously and shall provide relative time in seconds (2 second resolution) which will be

added to each data scan. The real-time clock shall be powered by internal batteries with a floating charge and shall operate continually during primary power interruptions up to 30 days.

4.4.6 Storage

The SDAS shall have the capability for tape storage of a minimum of 1.68 million bits (210 K bytes ± 10%) of data. The Random Access Memory (RAM) (used for temporary data storage and control program working space in the current design) has a minimum storage capability of 1 K bytes and the control program storage has a minimum storage capability of 6K bytes. The control program storage shall be a Programmable Read Only Memory (PROM). The control program shall accept data unique to the site for any number of measurements.

The SDAS shall utilize a magnetic tape to provide long term storage for the collected data.

The tape recording/playback technique used in the current design is a modification of Non-Return to Zero (NRZ). In this form of recording the magnetic coating is always magnetized to one state or the other, depending on whether a 1 or a 0 is to be recorded. With this continuous recording system, the magnetic coating is always magnetized in one direction or the other, thus erasure of previously recorded data is not required.

Tape Write/Read Timing

The tape write/read method selected for the current design (complemented NRZ-L) requires two tracks minimum. A 900 Hz clock is generated on the Tape/Command Card and data is presented to the Read/Write Amplifier Card as NRZ-L (see Figure 4.4.6-1). Track 1 is saturated in one polarity on the negative transition of the clock and is continuously saturated until the next "one" occurs during a negative clock transition. Track 2 operates similarly but remains saturated in one direction until the negative transition of the clock during a NRZ-L data "zero", then it is saturated in the other direction and remains so until another NRZ-L zero and negative clock transition occurs; then the direction of saturation changes again.

Recovery of data requires both tracks. Positive flux transitions on track 1 produce pulses, as shown on line 5, and negative transitions on track 1 produce pulses on line 6 from the read electronic circuits (reference Figure 4.4.6-1). Similarly, the R/W electronics produce pulses for positive track 2 transitions (line 7) and pulses for negative track 2 transitions (line 8). If lines 5 and 6 are "OR'ed", the result is shown on line 9, and if lines 7 and 8 are "OR'ed", the result is shown on line 10. NRZ-L data is recovered by triggering a Set-Reset Flip-Flop with the pulses shown on line 9 and on line 10. The OR of line 9 and 10 produces a 900 Hz pulse train related to the recovered NRZ-L data on line 11 and a clock is generated from this signal.

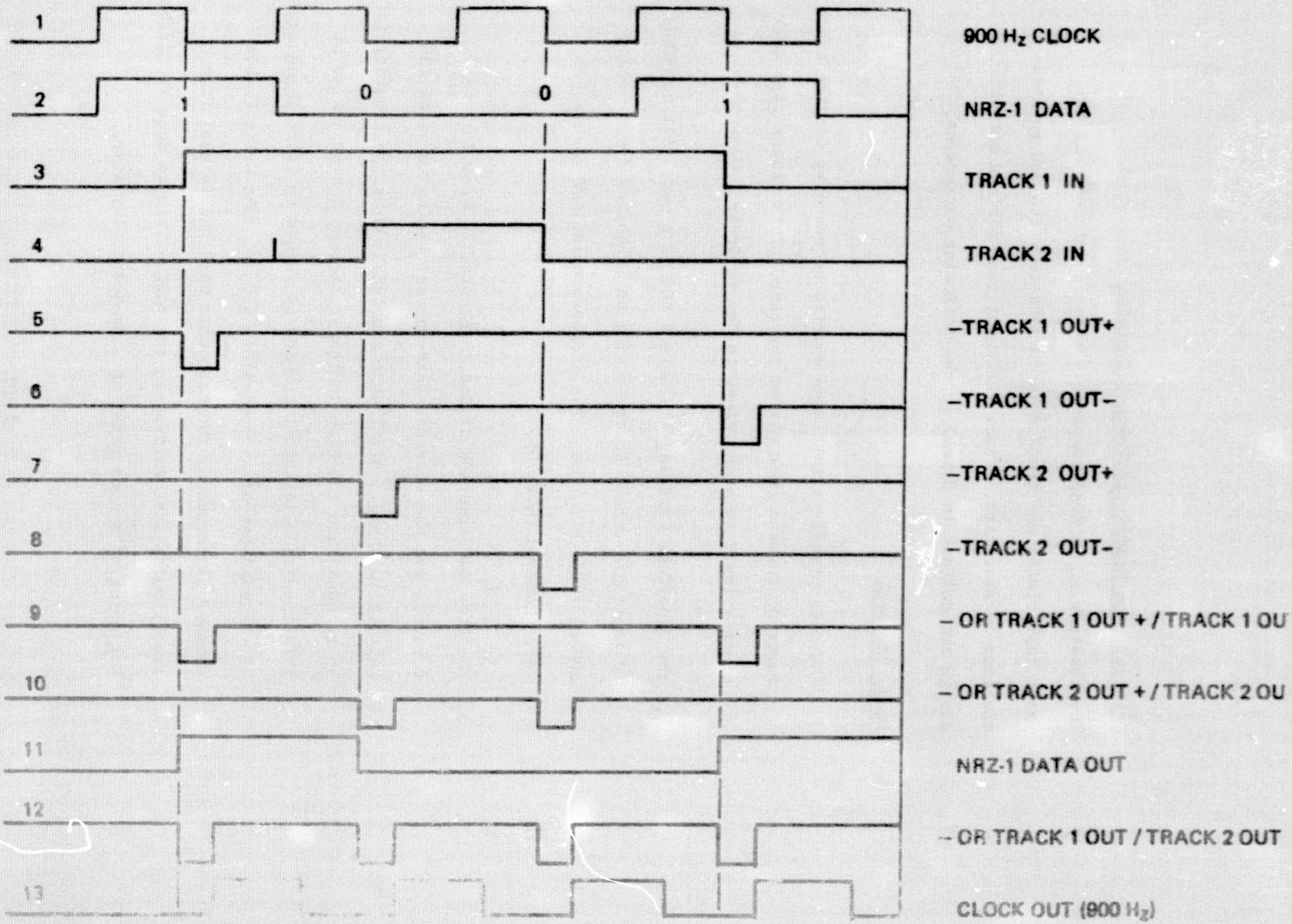

Figure A-1. Tape Recorder NRZ-1 Tape Record/Playback Timing

Critical Tape Read/Write Track Definition

The creation of an SDAS compatible tape is critical and the exact tape timing and track data formats to Write and to Read the tape is essential. These two operations for the current design are defined in detail in the following paragraphs.

Write (Record)

1. The microprocessor initiates a write sequence by issuing a Power On Command (Hex 80) to the tape. This causes tape deck control logic to bring power to the recorder.

2. The Tape/Comm Card logic starts a 600 ms timer. All commands to the logic except Power On will be inhibited for at least 600 ms from this time. The microprocessor now issues the Write Command (Hex 90).

3. The Stop Cmd (the NOR of Cmd. Reg. bits 1, 2, and 3) is removed, and the recorder take-up reel begins to bring the tape up to speed. After approximately 600 ms the recorder is up to speed and the Plan Indicator becomes active. Also at this time the Play-Start command is issued to start engagement of the head bar at approximately 850 ms. The Write Enable Command is issued by the Tape Comm Card and 16 dual (two track) pulses are written on the tape. This is done to indicate Beginning of Record (BER) in subsequent playbacks.

4. At this time the Full Empty (FLMT) Interrupt is issued which generates the Tape Interrupt to signal the microprocessor that the Serdes register is ready to accept the first byte of data. The Serdes register is a serial shift register that also has a parallel read/write feature.

5. Subsequent serial transfers of this register generate FLMT interrupts for parallel refills of the register until a data scan or record is completely written on the tape.

6. After the last byte has been sent to the Serdes Register, the microprocessor drops the Write Command by sending Power On (Hex 80). The tape logic writes 8 dual pulses, used during subsequent replays.

7. Finally the microprocessor issues stop (Hex 00) and the logic removes power from the recorder. As a result of the Tape/Comm Card logic receiving Stop, a Stop command is issued to the recorder Control Card and the Tape/Comm Card removes Write Enable to the Read/Write Card. The recorder coasts to a stop within approximately 100 ms with the record head disengaged (not touching the tape).

Read (Playback)

A read sequence is as follows (see Figure 4.4.6-2) with the assumption of the recorder is in an Inter-Record Gap (IRG).

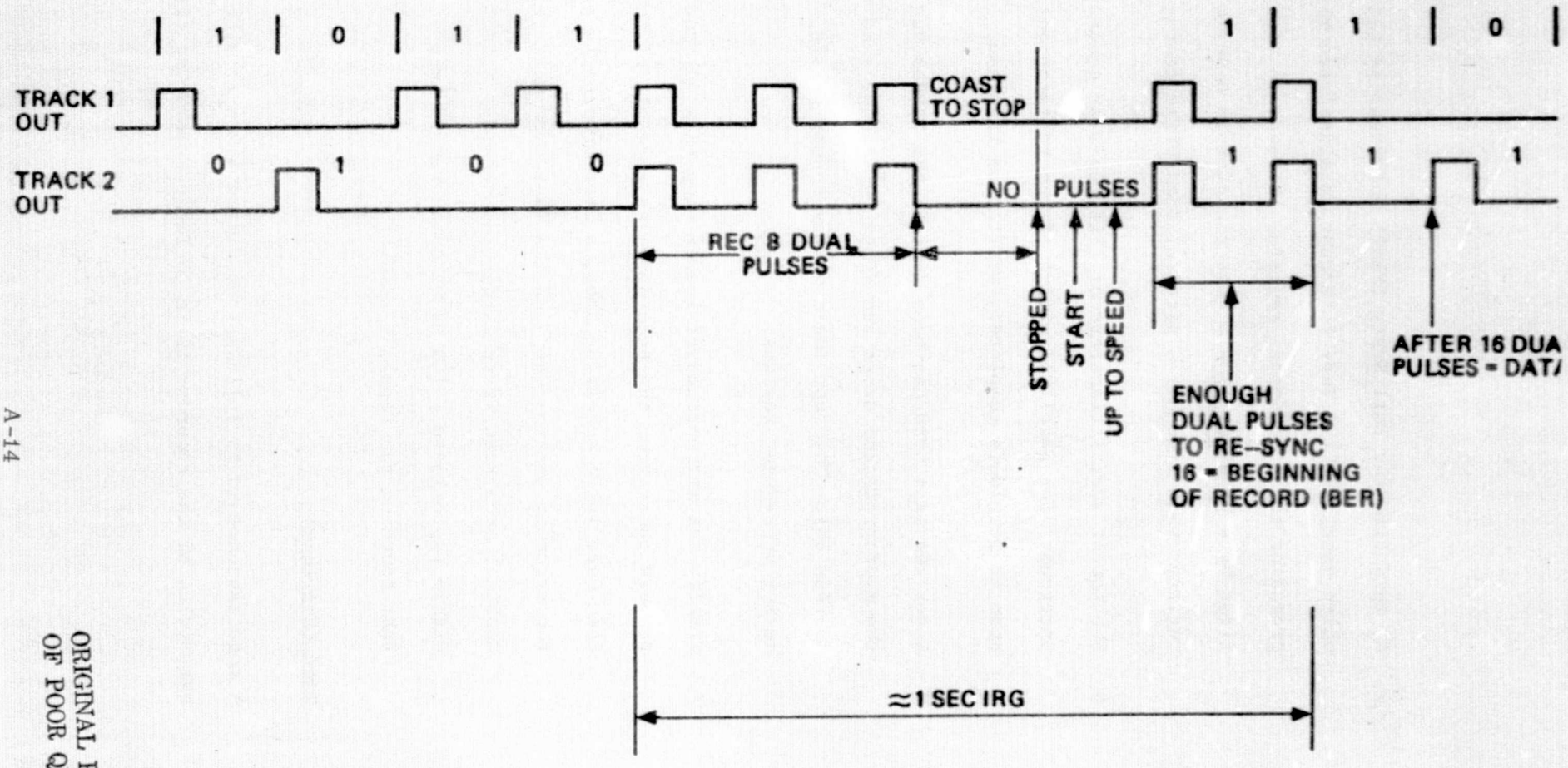

Figure 4.4.6-2. IRG Definition

1. The microprocessor issues Power-On (Hex 80) to the Cmd. Register. The 600 ms timer is activated and the Stop Command to the recorder is removed.

2. The microprocessor may now issue Read (Hex C0), but it will not be honored until 600 ms and data reads will further be delayed until the read head becomes engaged. Play Start was issued at approximately TBD ms and the Play Indicator became active at approximately 600 ms.

3. When the read head becomes engaged (approximately 850 ms after Power-On) serial pulses begin to be received. Normally, 16 of these pulses will be first received on both tracks and will be used to synchronize the derived 900 Hz clock and to look for the first data bits. As explained above all data will produce a pulse on one or the other tracks each clock time.

4. Operation proceeds with the recovered NRZ-L + clock being produced serially and clocked into the Serdes register until a FLMT interrupt causes it to be read into RAM memory and then sent to the communications channel for transmission to the control site.

5. When the tape logic detects an end of file, it will issue Stop (Hex 00) to the recorder.

6. In a commanded sequence, rewind would occur after the software had detected a unique bit pattern in the last record signifying End of File. If this occurs, the microprocessor would issue Rewind (Hex A0). After approximately 1 second the command is honored and the Rewind indicator is activated. Rewind continues with all heads disengaged until the tape deck senses the Beginning of Tape (BOT) holes in the tape. A stop is automatically issued by the recorder. The tape deck will allow coasting past BOT, restart in the forward direction, sense BOT and coast to a stop in the no data recorded space beyond BOT and issue BOT to the ISW to be read by the microprogram after rewind was commanded. Assuming the CDPS received a good transmission, it powers powers off the recorder by issuing Stop (Hex 00).

4.4.7 Power Supply

Three primary power supplies shall be provided in the SDAS; -24 vdc, +24 vdc, and +5 vdc. Other voltages required by the SDAS shall be generated "point-of-use" as required.

4.4.8 Data Retrieval

The collected data shall be both manually retrievable by physical removal of the tape or remotely retrievable via a standard voice-grade telephone line interface with the central site.

4.4.9 Data Rate and Format

The data stream shall be formatted for transmission over standard voice-grade telephone lines. The data transmission rate shall be 1.2 KBPS. The CDPS command message, SDAS reply message, SDAS data buffer (RAM Storage), SDAS tape and data transmission formats shall be provided as described below.

Figure 4.4.9-1 depicts the serial data recorded on the tape. Each scan contains the two LSB bytes of the SDAS Real Time Clock (RTC) followed by 6 data bytes, a BCH check byte; then repetitive blocks of 8 data bytes with their corresponding BCH (block check) byte until a complete scan is completed. Also contained in each record is one byte of SDAS station address, 3 bytes of the 24 bit RTC, and two bytes indicating the total number of bytes in the multiple scan record.

The total tape format is also shown. The CDPS is made aware of the number of records transmitted by software detection of the End-of-File pattern (11 bytes = FF, 6C, E0, 00, 00, 00, 0B, FF, FF, A4, FF).

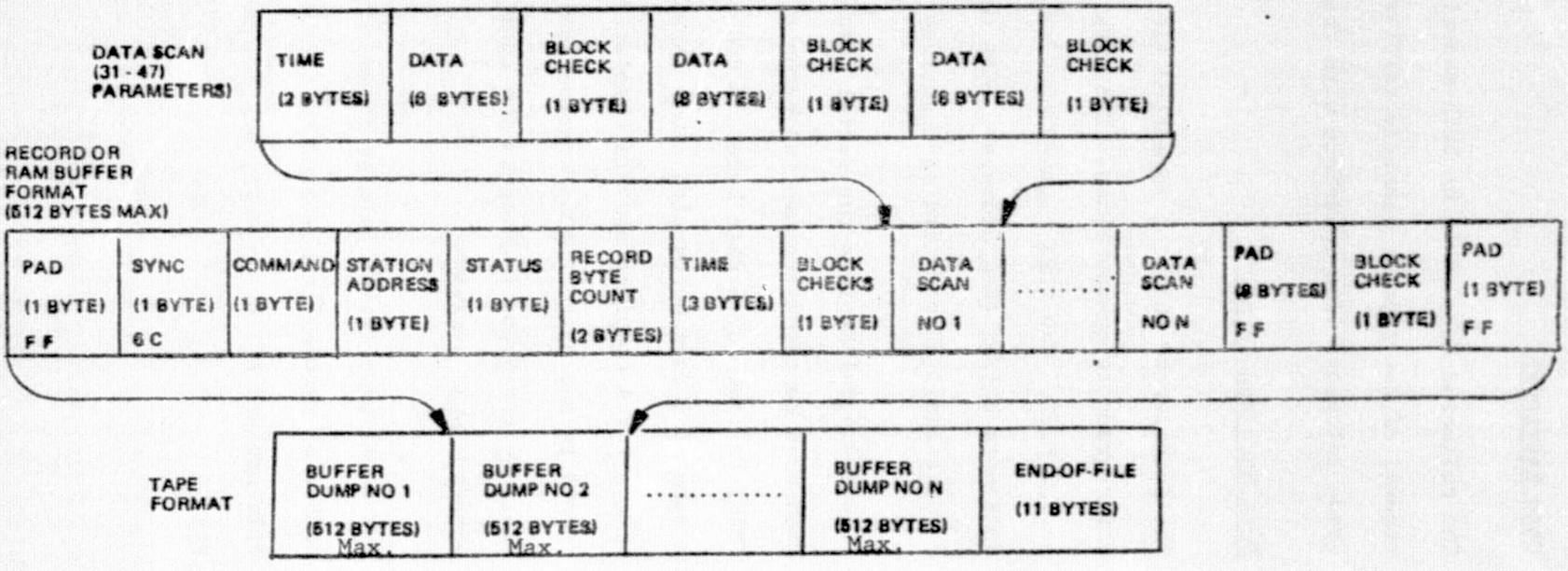

Figure 4.4.9-1. Tape Record Format

BCH Character

The block check character shall be a Bose-Chaudhuri-Hocquenghem (BCH) code derived byte that is calculated by the microcode in the SDAS and appended to each tape segment, usually 8 data bytes, before transmittal to the CDPS. The CDPS then compares the transmitted BCH byte against a BCH byte calculated from the received data, thereby determining if data bytes have been received that are in error. Examples of errors sources that shall be detected are SDAS tape recorder write/read, UART, and modem errors, telephone line errors (couplers, switching networks, etc.), and also errors in the CDPS receiving equipment.

The BCH check character, also called the Block check character, shall be calculated by the SDAS software using the polynomial $X^8 + X^7 + X^4 + X^3 + X + 1$. The following procedure is used to calculate the BCH check character.

1. Exclusive or the first character of each message frame whic[h] the contents of the BCH accumulator. (The BCH accumulator equals zero when the calculation begins.)

2. Shift the contents of the BCH accumulator one bit position to the left and test the condition of the high order bit (bit 0) as it shifts out of the accumulator.

If the high order bit shifts out as a zero, continue the shift left and test routine. If the high order bit shifts out as a one, exclusive-or the BCH accumulator with hexadecimal character 9B. Continue the shift and test routine until each of the 8 BCH accumulator bits has shifted left to the high order position and out for testing. This procedure must be followed for each character in each message frame. The BCH check character must be appended to the message frame for which it was calculated.

Figure 4.4.9-2 illustrates a flow chart of the BCH character calculation and Figure 4.4.9-3 represents an example of how a BCH check character is derived for the last frame of a message containing two characters, 39 and 01.

4.4.10 Scan Suspension

The SDAS shall not be required to collect data from the sensors while data is being transmitted to the CDPS site.

4.4.11 Error Detection

The SDAS shall suspend the collection and processing of sensor inputs when certain internal malfunctions are detected by the SDAS. It shall indicate this suspension when interrogated by the CDPS.

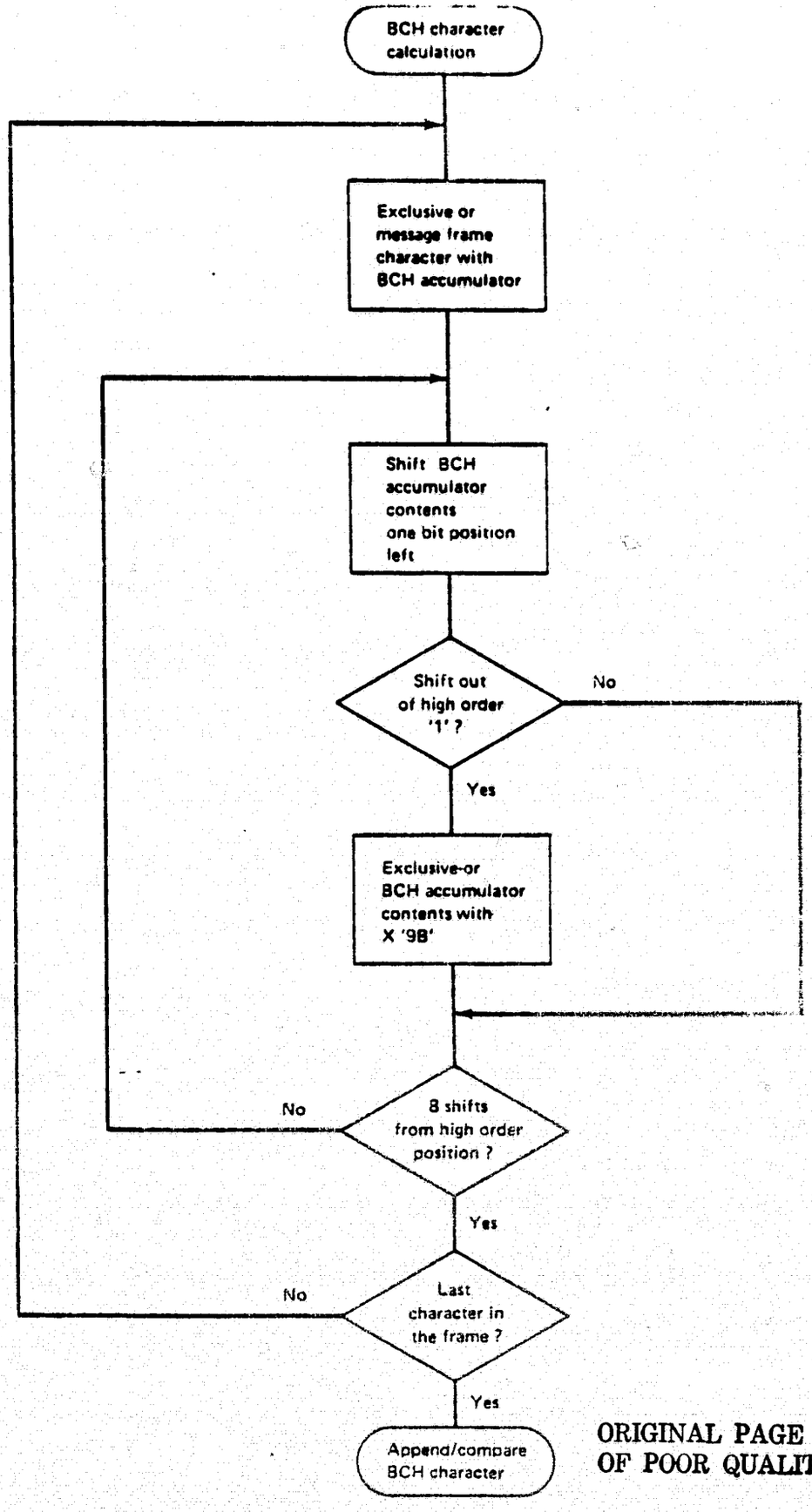

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Figure 4.4.9-2. Flowchart of BCH Check Character Calculation

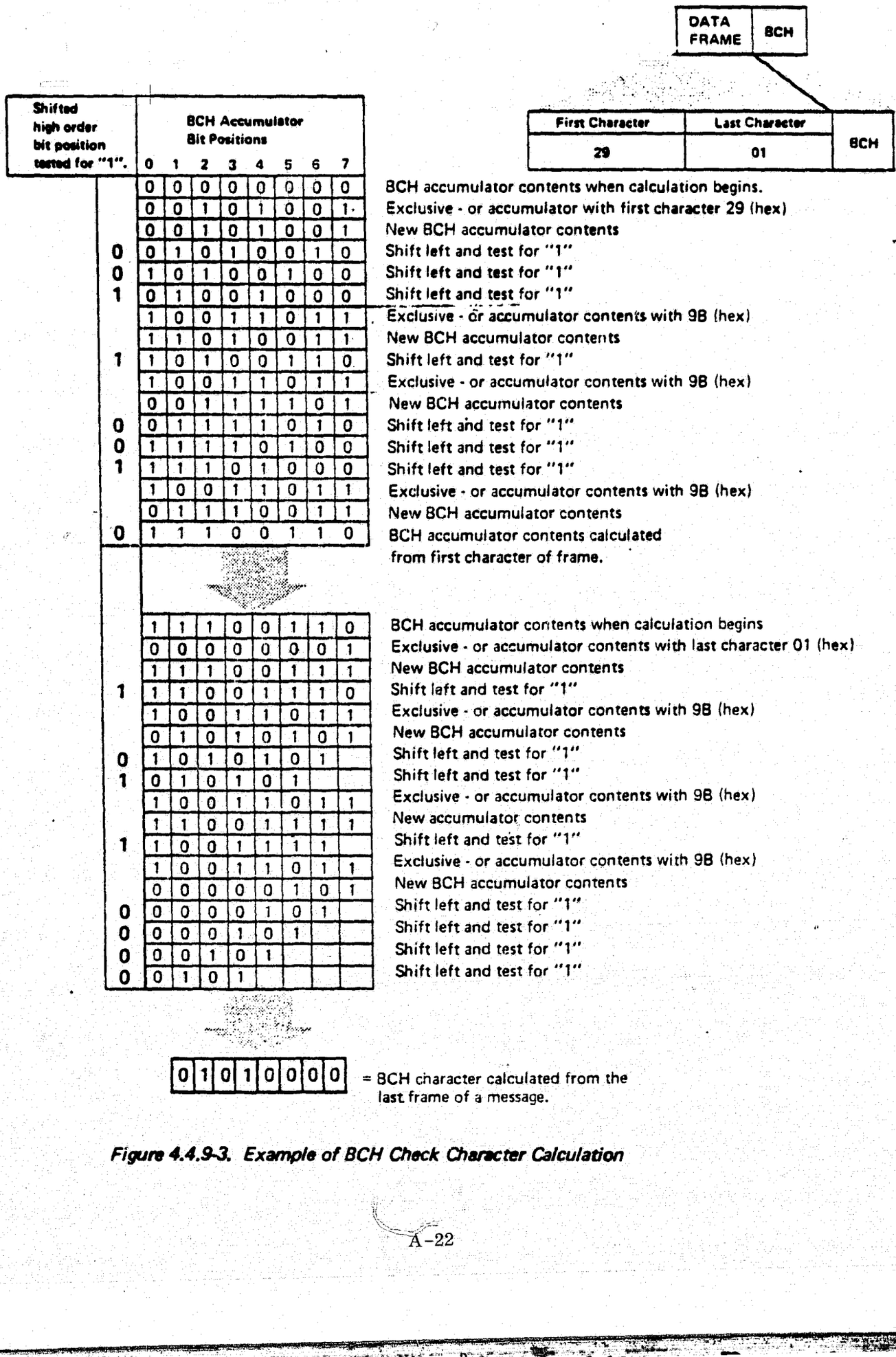


Figure 4.4.9-3. Example of BCH Check Character Calculation

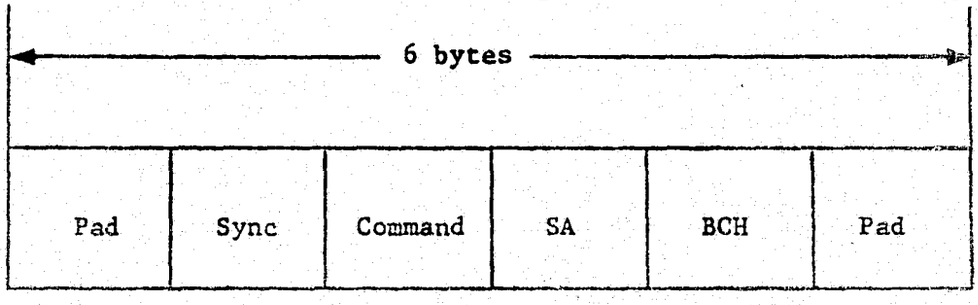
4.4.12 CDPS/SDAS Interface

The SDAS shall be capable of receiving and processing the CDPS commands, performing the indicated actions, and transmitting the reply information specified in Table 4.4-1.

The CDPS communication software initiates all communications between the CDPS and the SDAS. Each SDAS communication will begin with a command message to the SDAS and will be followed by a reply message from the site SDAS. Figure 4.4.12-1 illustrates the communications command/reply sequence necessary to collect data from a SDAS.

4.4.12.1 Commands to SDAS

All command messages shall have the following format:



Pad	-	FF	Circuit Activation Bits - 1 byte
Sync	-	6D	Synchronization byte
Command	-	HH*	Unique command code - see Table 4.4-1
SA	-	HH	Station Address - Selectable for each site
BCH	-	HH	Block Check Code for previous two bytes

*H - Hexadecimal Digit - 4 bits

Table 4.4-1. CDPS-SDAS Commands/Software Action

COMMAND TO SDAS AND HEX CODE	SDAS ACTION	REPLY ACTION
Read Configuration & End-of-File 'EF'	End of file written to tape cassette and reply message with current Realtime Clock (RTC) reading sent to CDPS	CDPS computes when SDAS RTC was initially "0" and proceeds to next command
Rewind 'AA'	Tape cassette is rewound and reply sent to CDPS	Reply message verified and next command issued
Read Tape 'E0'	Tape cassette is placed in play mode and data on cassette sent as reply message	Tape cassette data is read, BCH checked, & stored on disk
Disconnect '55'	Reply message sent to CDPS and SDAS disconnected from communications	Reply message verified - any new command must dial to reestablish communications with SDAS
Disconnect & Rewind '00'	Reply message sent to CDPS, SDAS disconnected from communications, and tape cassette rewound	Reply message verified - any new command must dial to reestablish communications with SDAS
Read Configuration* '2F'	Reply message sent to CDPS with current SDAS RTC reading	Reply message verified
Reinitialize** '1F'	Reply message sent to CDPS and a master reset of SDAS hardware and software executed	Reply message verified

*This command useful for verifying status of SDAS
**Not used during operational data collection

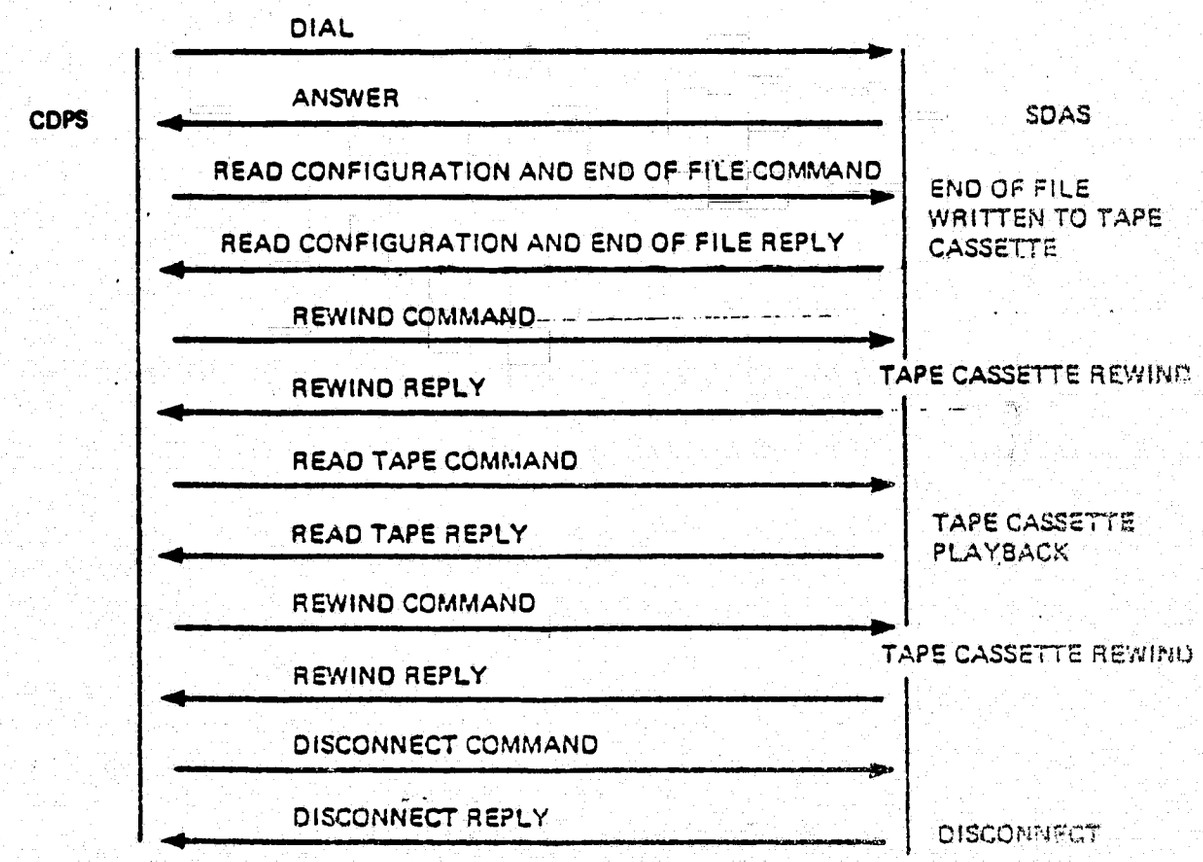


Figure 4.4.12-1. Command/Reply Sequence

4.4.12.2 Reply Messages from SDAS

A reply message shall be sent from the SDAS to the CDPS after every command message. Reply messages vary in length depending on the command received. The format of a reply message is defined in paragraph 4.4.12.3.

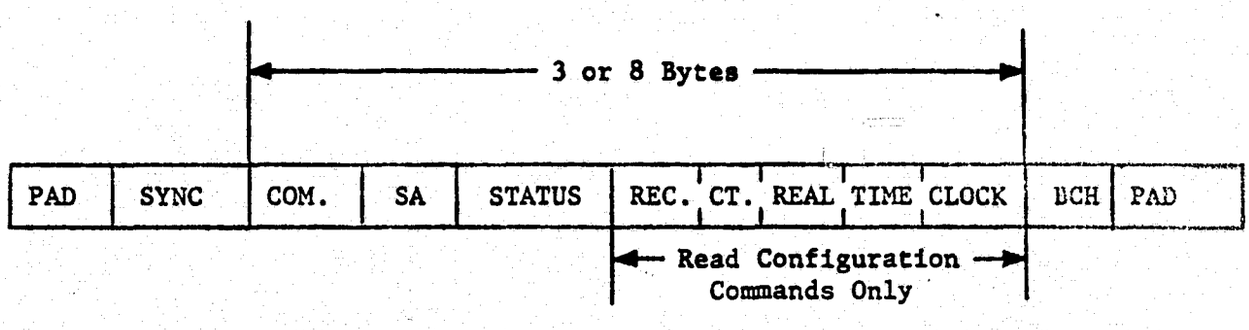
Two types of Reply Messages shall be provided by the SDAS:

Normal Reply Message - Bit 0 of the SDAS status code contains a "0".

Error Reply Message - Bit 0 of the SDAS status code contains a "1".

4.4.12.3 Reply Message Format

All reply messages with the exception of the Read Tape reply shall have the following format:



Pad	-	FF	Circuit Activation Byte - 1 byte
Sync	-	6C	Synchronization Byte
Command	-	HH*	Command Received - see Table 4.4-1. Same as command transmitted to SDAS
SA	-	HH	SDAS Station Address
Status	-	HH	SDAS Status - see paragraph 4.4.12.4
Record Ct.	-	HHHH	Unused
Real Time Clock	-	HHHHHH	24 Bit SDAS Real Time Clock Reading
BCH	-	HH	Block check clock for previous 3 or 8 bytes depending on reply

*H - Hexadecimal digit - 4 bits each

4.4.12.4 SDAS Status Information

The SDAS status shall be returned as part of the reply message as described above. The code shown below is unique to the current design SDAS. The intent of this requirement is that the SDAS error code shall isolate problems to the card level. The status codes for both normal and error replies have the following meaning:

SDAS Normal Reply

Code	Meaning
Hex 05	MPX 1 exists
Hex 06	MPX 1&2 exist
Hex 07	MPX 1, 2 & 3 exist

SDAS Error Reply

Code	Meaning
Hex 90	BCH error in command message
Hex 80	Invalid command received
Hex 01	Invalid station address received
Hex 84	Data Check
Hex C0	MPX 1 error
Hex C1	MPX 2 error
Hex C2	MPX 3 error
Hex C3	AI Basic error
Hex C4	Interval Timer error
Hex C5	Tape Control error
Hex C6	Real Time Clock error

4.4.12.5 SDAS/CDPS Timing Considerations

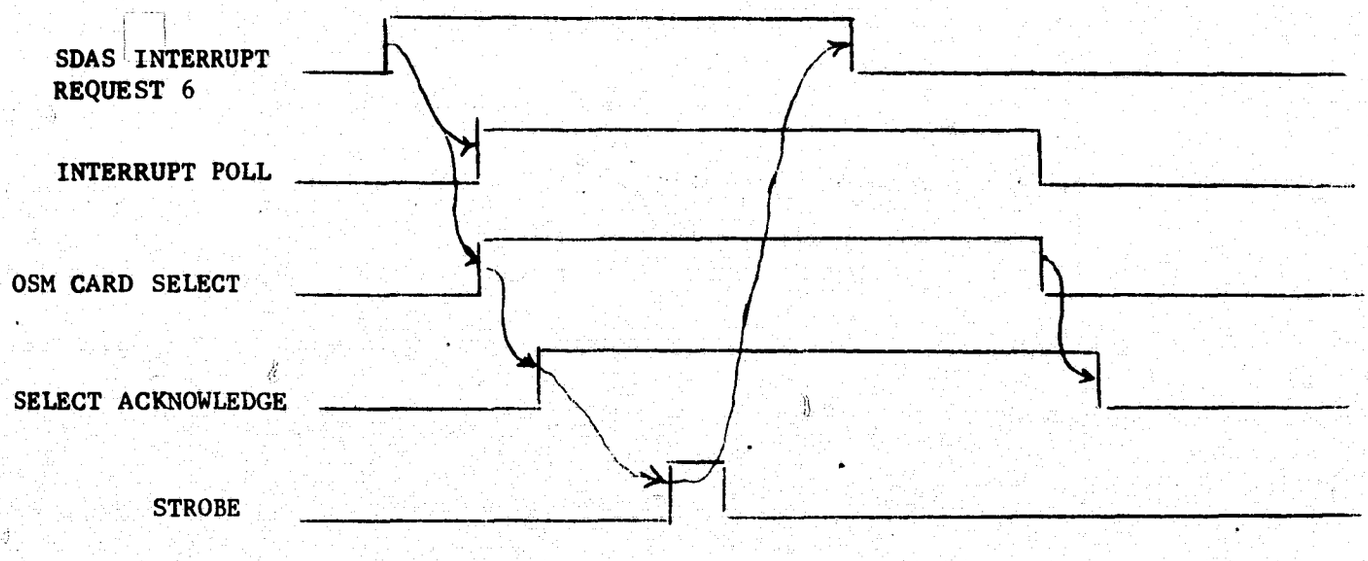
The CDPS must receive the first byte of the SDAS reply message within 37.5 seconds of the command message. Once the first byte of the SDAS reply message is sent, data must be sent at a rate exceeding one byte/second.

Upon loss of communications between the CDPS and the SDAS, the SDAS shall disconnect from the communication line.

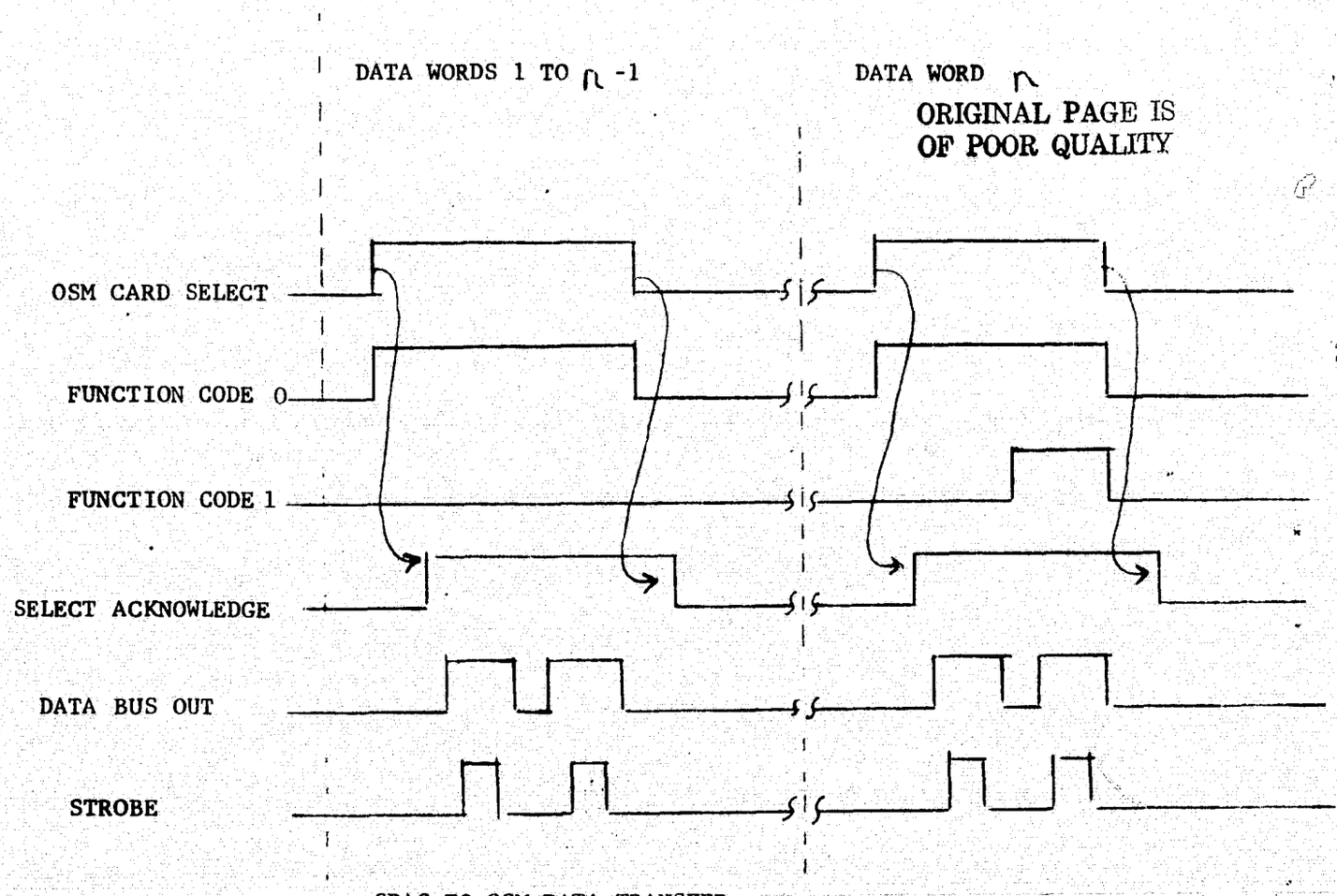
4.4.13 SDAS/OSM Interface

The SDAS shall be capable of accepting an interrupt from the On-Site Monitor (OSM) requesting data. In response to the request, the SDAS shall collect data from all input sensors being monitored, shall condition the data to a digital format, and shall transmit the digital data to the OSM. The SDAS shall then resume normal operations. The SDAS/OSM timing sequence required are shown in Figure 4.4.13-1.

SDAS-OSM COMMUNICATIONS



OSM SCAN REQUEST INTERRUPT



SDAS TO OSM DATA TRANSFER

Figure 4.4.13-1. Critical SDAS/OSM Sequences

4.4.14 SDAS-OSM Communications

The SDAS-OSM communications shall be accomplished via the OSM interface card located in the SDAS. The interface card shall be functionally transparent and allow the SDAS to communicate with the OSM I/O card. Communication is initiated by the OSM output called "SDAS Interrupt Request 6". This signal is a request for service and will result in a scan of sensor data being transmitted to the OSM. This request shall be acknowledged immediately by the SDAS, if it is not currently servicing another interface within the SDAS. If this condition exists, the request will be held off until the SDAS microprocessor is able to service the OSM.

The SDAS shall acknowledge the interrupt request by first issuing "Interrupt Poll" and "OSM Card Select". Receipt of "OSM Card Select" in the OSM causes the OSM to issue "Select Acknowledge". When the SDAS has received "Select Acknowledge" from the OSM, it shall issue the AI strobe pulse. This signals the OSM that the interrupt request has been acknowledged and that the SDAS is ready to initiate the data phase of the communications. Receipt of the "AI Strobe" in the OSM clears the interrupt request. The SDAS shall respond by removing "Interrupt Poll" and "OSM Card Select". Removal of "Card Select" causes the OSM to remove "Select Acknowledge."

The data phase of the communications shall proceed with the SDAS microprocessor reading a sensor channel, compensating the data for known null offsets and packing the resultant data into two 8 bit words for transfer to the OSM. The 10 bits of sensor data shall be packed in the 8 bits of the first word and bit 0 and 1 of the second word. Bit 0 of the first word is the MSB.

Transfer of the data shall be accomplished by the SDAS issuing "OSM Card Select" and "Function Code 0". The "OSM Card Select" signal causes the OSM to respond with "Select Acknowledge". Upon receipt of "Select Acknowledge", the SDAS shall put the first word on the "Data Out Bus" and issue the "AI Strobe" when the data is stable. The "AI Strobe" signal loads the data into the OSM data input register. Approximately 10 μ sec later the SDAS shall put the second word on the "Data Out Bus" and issue the "AI Strobe" to load the data in the OSM. The SDAS shall then remove "OSM Card Select" and the OSM responds by removing "Select Acknowledge". This completes the transfer of one channel of sensor data. This process shall be repeated until all channels have been read and transmitted to the OSM. The one exception is the signal called "Function Code 1". This signal shall be issued by the SDAS prior to transmitting the last word of the last channel of data. This alerts the OSM that the SDAS-OSM communications are complete.

4.5 SDAS INTERFACES

4.5.1 Interface Description

The SDAS shall provide interfaces for connection to the sensors, power and telephone lines, and on-site monitor (see Figure 4.5.1-1 for a functional block diagram).

4.5.2 SDAS Primary Power

Power to the SDAS shall be standard 110-125 V, 60 Hertz, 1 PHASE 3 amps service. A standard 3 wire interface (safety ground, power and return) shall be required.

4.5.3 Telephone

The SDAS shall interface with standard Bell System CBS Data Sets Access Arrangement Series 5 or later, or equivalent. The SDAS modem shall operate at 1200 BPS and shall be designed to interface with a Bell Data Set 202-C and -D.

4.5.4 Sensor Interface

The SDAS shall provide the capability to accept data from a maximum of 95 sensors and to interface with the sensors via internal pluggable microboards (one per channel) or other signal conditioning electronics.

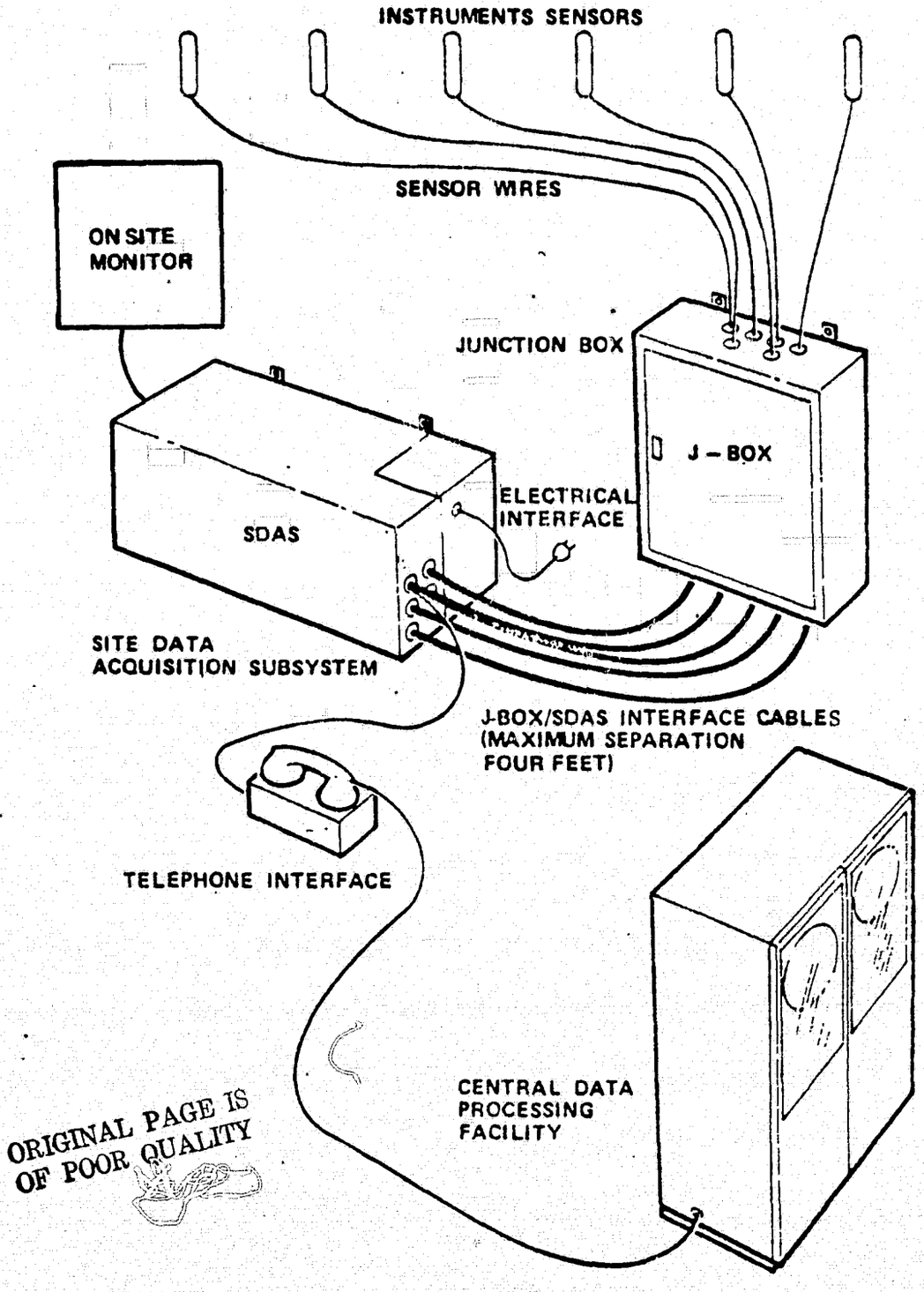


FIGURE 4.5.1-1.
SITE INSTRUMENTATION INTERFACE HARDWARE CURRENT DESIGN 48 CHANNEL UNIT

4.5.4.1 Signal Conditioning Interface

The signal conditioning card(s) included in the SDAS shall provide the capability to be easily configured for particular sensor combinations. The current design SDAS uses the pluggable signal conditioning microboards described in Appendix 1. Typical voltage range and signal gain assignments for each input channel (48 channel unit) are given in Table 4.5-1. The SDAS shall accept inputs in either the 0-5 vdc or 0-100 mvdc range and provide either 1 or 50 gains on each channel to provide 0-5 vdc output to the A/D converter.

4.5.4.2 Sensor Power Requirements

The SDAS shall provide a limited amount of power for use by the attached sensors. Signal conditioning electronics shall be capable of supplying the following power for use by sensors:

+15 vdc	12.0 watts (800 ma)
+3.6 vdc	.144 watts (40 ma)
+5 vdc	5.0 watts (1000 ma)

These levels are the maximum capability of the electronics. Power utilized by the sensor signal conditioning electronics is considered as power supplied to the sensor and must be accounted for in computing the total power required by the sensor.

Table 4.5-1. SDAS I/O Pin Function and Channel Allocation

I/O Conn. No. J	Sensor Channel or Function	No. I/O Wires	I/O Pin Numbers Hi	Lo	3rd	Input Voltage Acceptable	SDAS Amp Gain	Data Bits Stored	Mux No.	S/C Card No.
101	1	2	-	-	(Offset Meas. - Internal)				1	1
101	2(A)	3	3	4	5	0-100 mv	50	10	1	1
101	3(A)	2	9	10	-	0-100 mv	50	10	1	1
101	4(A)	3	7	8	6	0-100 mv	50	10	1	1
101	5(A)	2	13	14	-	0-100 mv	50	10	1	1
101	6(A)	3	15	16	17	0-100 mv	50	10	1	1
101	7(A)	2	21	22	--	0-100 mv	50	10	1	1
101	8(A)	3	19	20	18	0-100 mv	50	10	1	1
101	9	2	25	26	-	0-100 mv	50	10	1	1
101	10	3	27	28	29	0-100 mv	50	10	1	1
101	+5 vdc	1	11	-	-				-	1
101	+3.6 vdc	1	32	-	-				-	1
101	+15 vdc	1	30	-	-				-	1
101	Ground	2	31	12	-				-	-
101	Shield	1	37	-	-				-	-
101	Spare	3	23	24	33				-	-
101	Spare	3	1	2	-				-	-
101	Spare	3	34	35	36				-	-
102	11	2	1	2	-	0-100 mv	50	10	1	1
102	12	3	3	4	5	0-100 mv	50	10	1	1
102	13	2	9	10	-	0-100 mv	50	10	1	1
102	14	3	7	8	6	0-100 mv	50	10	1	1
102	15	2	13	14	-	0-5 v	1	10	1	1
102	16	3	15	16	17	0-100 mv	50	10	1	1
102	17	2	21	22	-	0-100 mv	50	10	2	1
102	18	3	19	20	18	0-100 mv	50	10	2	1
102	19	2	25	26	-	0-100 mv	50	10	2	1
102	20	3	27	28	29	0-100 mv	50	10	2	1
102	21	2	31	32	-	0-100 mv	50	10	2	1

(A) = Asynchronously Sampled

Table 4.5-1. SDAS I/O Pin Function and Channel Allocation (Continued)

I/O Conn. No. J	Sensor Channel or Function	No. I/O Wires	I/O Pin Numbers Hi	Lo	3rd	Input Voltage Acceptable	SDAS Amp Gain	Data Bits Stored	Mux No.	S/C Card No.
102	+3.6 vdc	1	23							
102	+15 vdc	1	24							
102	+5 vdc	1	11	-	-				-	1
102	Ground	1	12	-	-				-	-
102	Shield	1	37	-	-				-	-
102	Spare	2	35	36	-				-	-
103	23	2	1	2	-	0-100 mv	50	10	2	1
103	24	3	3	4	5	0-100 mv	50	10	2	1
103	25	2	9	10	-	0-100 mv	50	10	2	1
103	26	3	7	8	6	0-100 mv	50	10	2	1
103	27	2	13	14	-	0-100 mv	50	10	2	1
103	28	3	15	16	17	0-100 mv	50	10	2	1
103	29	2	21	22	-	0-100 mv	50	10	2	1
103	30	3	19	20	18	0-100 mv	50	10	2	1
103	31	2	25	26	-	0-5 v	1	10	2	1
103	32	3	27	28	29	0-100 mv	50	10	2	1
103	+5 vdc	1	11	-	-			-	-	1
103	+3.6 vdc	1	32	-	-			-	-	1
103	+15 vdc	1	30	-	-			-	-	1
103	Ground	2	12	31	-			-	-	-
103	Shield	1	37	-	-			-	-	-
103	Spare	3	23	24	33			-	-	-
103	Spare	3	34	35	36			-	-	-

Table 4.5-1. SDAS I/O Pin Function and Channel Allocation (Continued)

I/O Conn. No. J	Sensor Channel or Function	No. I/O Wires	I/O Pin Numbers Hi	Lo	3rd	Input Voltage Acceptable	SDAS Amp Gain	Data Bits Stored	Mux No.	S/C Card No.
104	33(A)	2	1	2	-	0-100 mv	50	10	3	2
104	34(A)	3	3	4	5	0-100 mv	50	10	3	2
104	35(A)	2	9	10	-	0-100 mv	50	10	3	2
104	36	3	7	8	6	0-100 mv	50	10	3	2
104	37	2	13	14	-	0-100 mv	50	10	3	2
104	38	3	15	16	17	0-100 mv	50	10	3	2
104	39	2	21	22	-	0-100 mv	50	10	3	2
104	40	3	19	20	18	0-100 mv	50	10	3	2
104	41	2	25	26	-	0-5 v	1	10	3	2
104	42	3	27	28	29	0-100 mv	50	10	3	2
104	+5 vdc	1	11	-	-			-	-	2
104	+3.6 vdc	1	32	-	-			-	-	2
104	+15 vdc	1	30	-	-			-	-	2
104	Ground	2	12	31	-			-	-	-
104	Shield	1	37	-	-			-	-	-
104	Spare	6	23	24	33			-	-	-
104	Spare	6	34	35	36			-	-	-
105	43	3	1	2	3	0-100 mv	50	10	3	2
105	44	3	5	6	4	0-100 mv	50	10	3	2
105	45	3	9	10	11	0-100 mv	50	10	3	2
105	46	3	13	14	12	0-100 mv	50	10	3	2
105	47	3	17	18	19	0-100 mv	50	10	3	2
105	48	3	21	22	20	0-100 mv	50	10	3	2
105	+5 vdc	1	7	-	-	-	-	-	-	2
105	+3.6 vdc	1	15	-	-	-	-	-	-	2
105	+15 vdc	1	23	-	-	-	-	-	-	2
105	Ground	2	8	16	-	-	-	-	-	-
105	Shield	1	28	-	-	-	-	-	-	-
105	Ring Indicator	1	30	-	-	-	-	-	-	-

Table 4.5-1. SDAS I/O Pin Function and Channel Allocation (Continued)

I/O Conn. No. J	Sensor Channel or Function	No. I/O Wires	I/O Pin Numbers Hi	Lo	3rd	Input Voltage Acceptable	SDAS Amp Gain	Data Bits Stored	Mux No.	S/C Card No.
105	Data Modem Ready	1	31	-	-	-	-	-	-	-
105	Switch Hook	1	32	-	-	-	-	-	-	-
105	Off Hook	1	33	-	-	-	-	-	-	-
105	Coupler Cut Through	1	34	-	-	-	-	-	-	-
105	Coupler Ground	1	35	-	-	-	-	-	-	-
105	Data Ring	1	36	-	-	-	-	-	-	-
105	Data Tip	1	37	-	-	-	-	-	-	-
10	Spare	3	24	25	26	-	-	-	-	-
105	Spare	2	27	29	-	-	-	-	-	-

Table 4.5-1. SDAS I/O Pin Function and Channel Allocation (Continued)

PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
01	-OSM TO SDAS DBI BIT 0	18	SUBADDRESS BIT 0
02	1	19	1
03	2	20	2
04	3	21	3
05	4	22	SDAS TO OSM DBO BIT 0
06	5	23	1
07	6	24	2
08	7	25	3
09	-CARD SELECT 2	26	4
10	-INTERRUPT POLL	27	5
11	-OSM INTERRUPT REQUEST	28	6
12	-OSM SELECT ACK	29	7
13	-AI STROBE	30	-SYSTEM RESET
14	FUNCTION BIT 0	31	-CLOCK
15	1	32	-OSM CONNECTED
16	2	33	
17	3	34	
		35	
		36	
		37	

4.5.5 Detailed SDAS Physical Interfaces

The SDAS shall provide ten 37-pin connectors for connection with the sensors and the telephone interfaces, and a 3-wire power cord for power interface. The SDAS I/O connector pin function assignments for the first 47 sensor inputs and power outputs are given in Table 4.5-1. The second 48 channels shall have the same pin functions except that there shall be no offset measurement. The SDAS shall provide one 37-pin connector for the OSM interface.

4.6 PACKAGING

4.6.1 Design Environment

The SDAS shall be designed to operate in an indoor environment having temperature extremes between $32^{o}F$ and $100^{o}F$ and relative humidity limits of 5% to 80% without condensation.

4.6.2 Modularity

The SDAS shall be designed using modular elements.

4.6.3 Mounting

The SDAS shall be wall mounted by 1" square brackets at the top back and bottom back of the SDAS with mounting holes 16" apart, both top and bottom. Either molly bolts, wood screws or bolt/nut combination will be used to mount the unit to the mounting surface, depending on the characteristics of the mounting surface.

Maximum weight of the SDAS shall be 75 pounds, and its dimensions shall not exceed 36" x 18" x 12".

4.7 DESIGN AND CONSTRUCTION

4.7.1 Wiring

All subsystem wiring shall be in compliance with the 1976 National Electric Code.

4.7.2 Failure Protection

UL recognized circuit protection devices shall be used to provide fault isolation, wiring protection, and shall protect against short circuits. These devices shall comply with the UL code in effect on April 30, 1976.

4.7.3 Grounding

Grounding of all electrical/electronic circuitry shall be in accordance with the applicable 1976 National Electric Code.

4.7.4 Component Selection

The electrical and mechanical design shall utilize at least commercial grade components.

4.7.5 Fungi/Mildew Resistance

Components of the system shall not support the growth of fungi, mold, and/or mildew in the presence of moisture to an extent that will impair their operational function over their intended service life.

4.7.6 Materials Compatibility

Component materials used in the subsystem shall be selected to minimize corrosion and deterioration that could degrade component performance under operating conditions.

4.7.7 Dissimilar Materials

Dissimilar materials and dissimilar materials coated with corrosion resistant finishes when used in contact with each other shall not create corrosive deterioration which interferes with mechanical or electrical performance of the SDAS or its associated parts.

4.7.8 Interchangeability

Mechanical and electrical interchangeability and replaceability for a particular design of the SDAS shall exist in form, fit, and function of assemblies and subassemblies.

4.7.9 Marking

Marking of the systems shall be in accordance with good commercial practices in order to facilitate assembly, checkout and maintenance. MSFC shall provide name plates for installation on the finished SDAS by the manufacturer.

4.7.10 Workmanship

Workmanship in fabrication and assembly of the SDAS shall be consistent with good commercial practice. The noise level of the SDAS shall be as quiet as possible.

4.7.11 Safety

The SDAS shall be certified in a reasonable time and shall meet UL requirements in effect on April 30, 1976.

4.7.12 Fire Prevention

The SDAS shall conform to the fire section of applicable national fire codes in effect on April 30, 1976.

4.8 RELIABILITY/MAINTAINABILITY

4.8.1 Maintenance/Replaceable Units

The SDAS shall be of a modular design to permit replacement of failed subassemblies.

4.8.2 Accessibility

The SDAS shall be designed to assure that field replaceable items shall be accessible for servicing, removal or replacement.

4.8.3 Reliability

The SDAS shall use commercial grade components and shall be designed not to adversely affect the operation and performance of the monitored system.

4.8.4 Serviceability

The SDAS shall be capable of being serviced with a minimum amount of special equipment by a trained field technician.

5.0 GEORGRAPHICAL AREA

The SDAS shall be capable of operating in any geographical area in the United States subject to the restrictions specified elsewhere in this document.

APPENDIX 1

SIGNAL CONDITIONING CIRCUITS

1.0 INTRODUCTION

This appendix defines the signal conditioning circuits required for each sensor. (Microboard circuits which plug into the SDAS signal conditioning card and which are used to condition the sensor inputs to interface with the SDAS multiplexer card(s) are used for the current design SDAS.)

2.0 SENSOR INTERFACE AND MICROBOARD REQUIREMENTS

Table 1-1 lists sensor interface characteristics required to interface these sensors with the SDAS. (Microboard configurations used in the current design SDAS are also shown).

Table 1-1. Sensor Interface Requirements

CHANNEL UTILIZATION	SENSOR INPUT	SENSOR OUTPUT	SDAS AMPLIFIER GAIN	NO. WIRES	MICROBOARD TYPE
Pyranometer	-----	0-15 mvdc	50	2 + S	Straight Through
Resistance Thermal Detector (RTD)	+15 vdc 15 ma	0-100 mvdc	50	2/3 + S	Temperature Bridge
Delta RTD	+15 vdc 20 ma	0-100 mvdc	50	3 + S	Delta Temperature Bridge
Target Type Flowmeter	+5.0 vdc 20 ma	0-10 mvdc	50	4 + S	Straight Through
Hot Wire Anonometer	115 vac	0-5 vdc	1	2 + S	Straight Through or Voltage Divider
Wattmeter	-----	0-150 mvdc	50	2 + S	Straight Through or Voltage Divider
Humidity	+3.6 vdc 10 ma	0-100 mvdc	50	4 + S	Straight Through
Wind Speed	-----	13.3 vdc @ 100 mph	1	2 + S	Voltage Divider
Wind Direction	+5 vdc 10 ma	0-5 vdc	1	3 + S	Straight Through or Voltage Divider
Unused Channels	-----	-----	--	-----	Input Shorting

3.0 SENSOR SIGNAL CONDITIONING MICROBOARDS

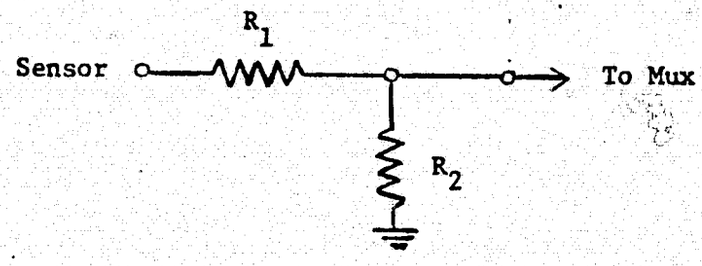
The following signal conditioning circuits shall be provided. For the current design SDAS, four standard types of signal conditioning circuits are mounted on pluggable microboards which plug into mounting sockets included on the SDAS signal conditioning cards. The microboard types for each acceptable sensor are shown in Table 1-1. All channels now have pluggable microboards for mounting signal conditioning circuitry. Any microboard is pluggable in any channel.

3.1 STRAIGHT THROUGH WIRING

Analog or digital discrete inputs of 0 to 5 vdc or 0 to 100 millivolts dc shall not require conditioning. (Microboards wiring the sensor input directly to the multiplexer input are provided for the current design SDAS.)

3.2 DIVIDER NETWORK

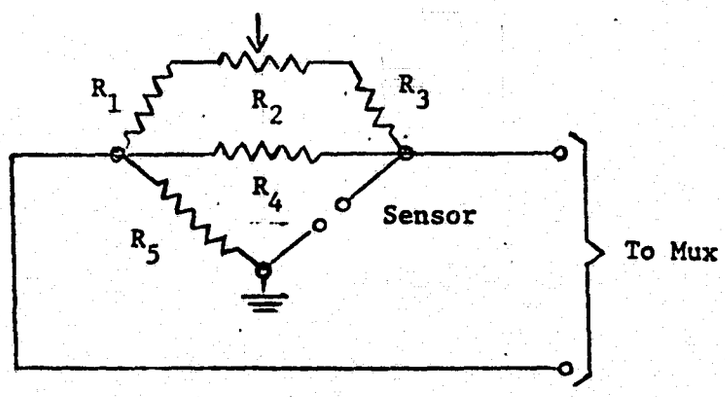
A divider network shall be provided as shown below to condition sensor outputs to 0-5 vdc or 0-100 mvdc as specified in Table 1-1. (A pluggable microboard is used for the current design SDAS.)



NOTE: The specific voltage values are dependent upon the range of the input and output voltages and shall be selected to maximize output values. Currently selected divider networks include 9:1, 2:1 and 49:1 values for $R_1:R_2$.

3.3 TEMPERATURE BRIDGE

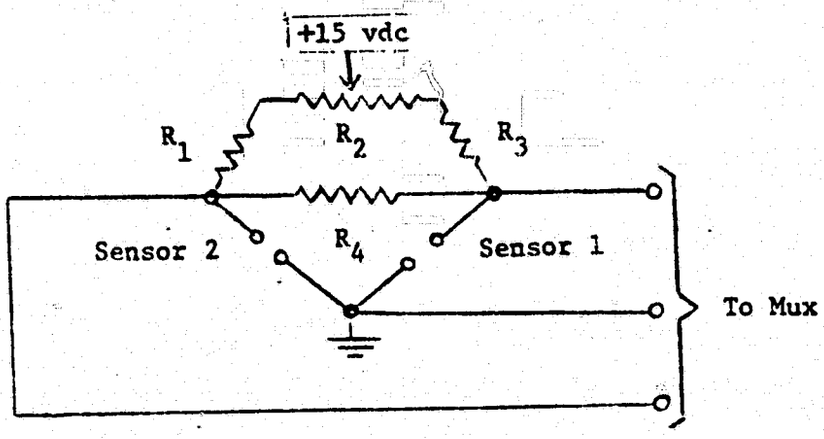
Analog inputs from a 100 ohm resistance thermal detector shall be conditioned to a 0 to 100 mvdc output using the following circuit. (The circuit is mounted on a pluggable microboard for the current design SDAS.)



NOTE: The specific resistor values are dependent on the range of the input temperature being measured and shall be selected to meet performance evaluation accuracy requirements. Temperature range values selected for implementation include 30°F to 230°F, 30°F to 160°F, 30°F to 450°F, and -20°F to 120°F.

3.4 DELTA TEMPERATURE BRIDGE

Analog inputs from 100 ohm resistance thermal detectors used to measure differential temperatures shall be conditioned to a 0 to 100 mvdc output using the following circuit. (The circuit is mounted on a pluggable microboard for the current design SDAS.)



NOTE: The specific resistor values are dependent on the range of the input delta temperature being measured and the base value of the temperature from which the delta temperature is being measured, and shall be selected to meet performance evaluation accuracy requirements. Delta temperature range values and base for delta temperature selected for implementation include -10°F to 50°F (100°F base), 0°F to 100°F (75°F base), 0°F to 80°F (75°F base), and 0°F to 25°F (150°F base).

3.5 INPUT SHORTING NETWORK

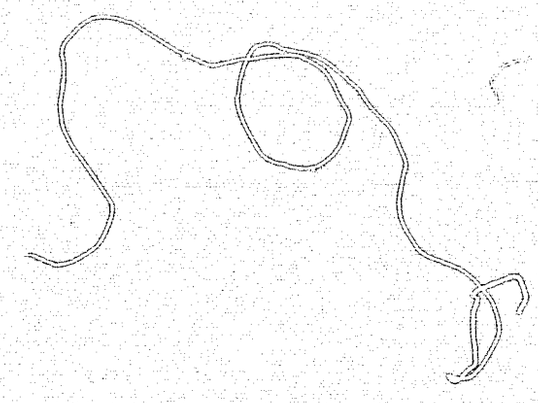
Provision shall be made to tie the high and low input signals together for input channels which are read by the microprocessor, but which have no sensor input on the channel. (A pluggable microboard is provided for the current design SDAS.)

SECTION B

SITE DATA ACQUISITION SUBSYSTEM

MICROPROGRAM

DESCRIPTION DOCUMENT



1. SDAS MICROPROGRAM DESCRIPTION

The SDAS Microprogram consists of the software which resides in the SDAS Microprocessor and performs the following functions:

(1) Microprocessor Power-On/Reset
(2) Software/Hardware Initialization
(3) SDAS Hardware Configuration Determination
(4) Microprocessor Interrupt Handling
(5) Hardware/Software Error Handling
(6) Time Keeping
(7) S/7-SDAS Communication Processing
(8) Reading of Sensor Input
(9) Recording of Data on Tape/Tape Control
(10) On-Site Monitor/On-Site Display Support

The structure of the Microprocessor is shown in Figure 1. As can be seen, entry to the program is via a Microprocessor power-on or reset signal. Control of the program is performed by a "Control Program" which calls the appropriate application program for execution. Details of the software elements shown in the figure are presented in subsequent sections of this document.

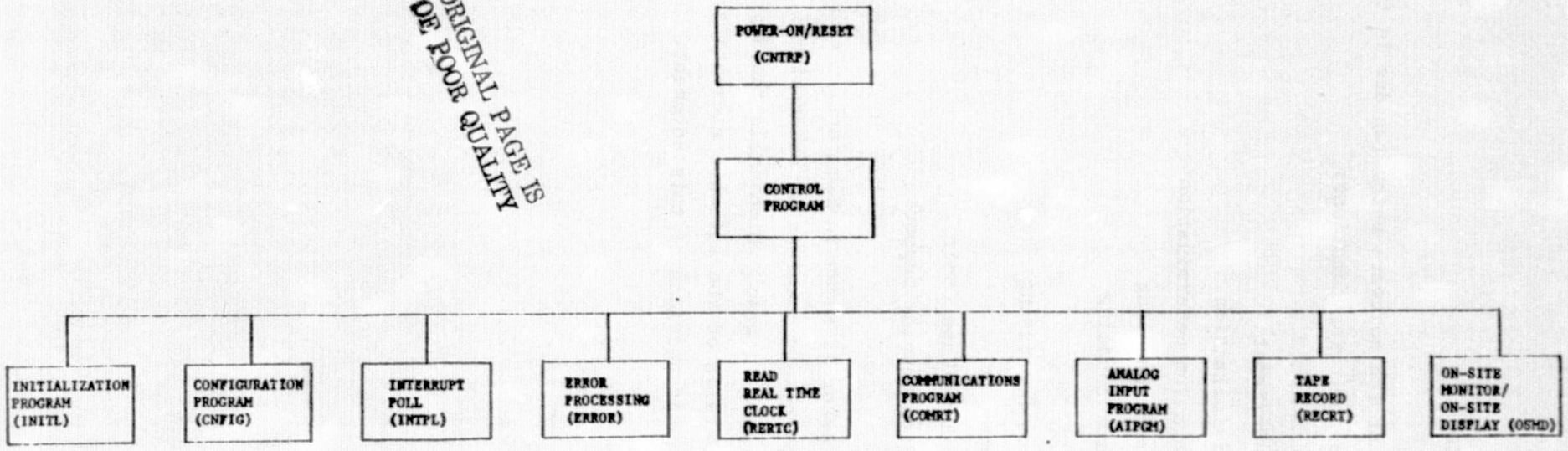


Figure 1. SDAS Microprogram Structure

2. POWER-ON/RESET - CONTROL PROGRAM

Upon receipt of a "Power-On/Reset" signal, the Microprocessor logic forces the software to location "000" for initialization purposes. The Microprocessor enters the Power-On/Reset logic as shown in Figure 2. After initialization and configuration functions are performed, the program is driven by the occurrence of external interrupt indicators. The Interrupt Poll Program (INTPL) continuously monitors the Microprocessor's Interrupt Register, polls the hardware for the Interrupt Status Word (ISW) and transfers control to the appropriate program. Once an application program is initiated, it must be completed prior to initiation of another application program.

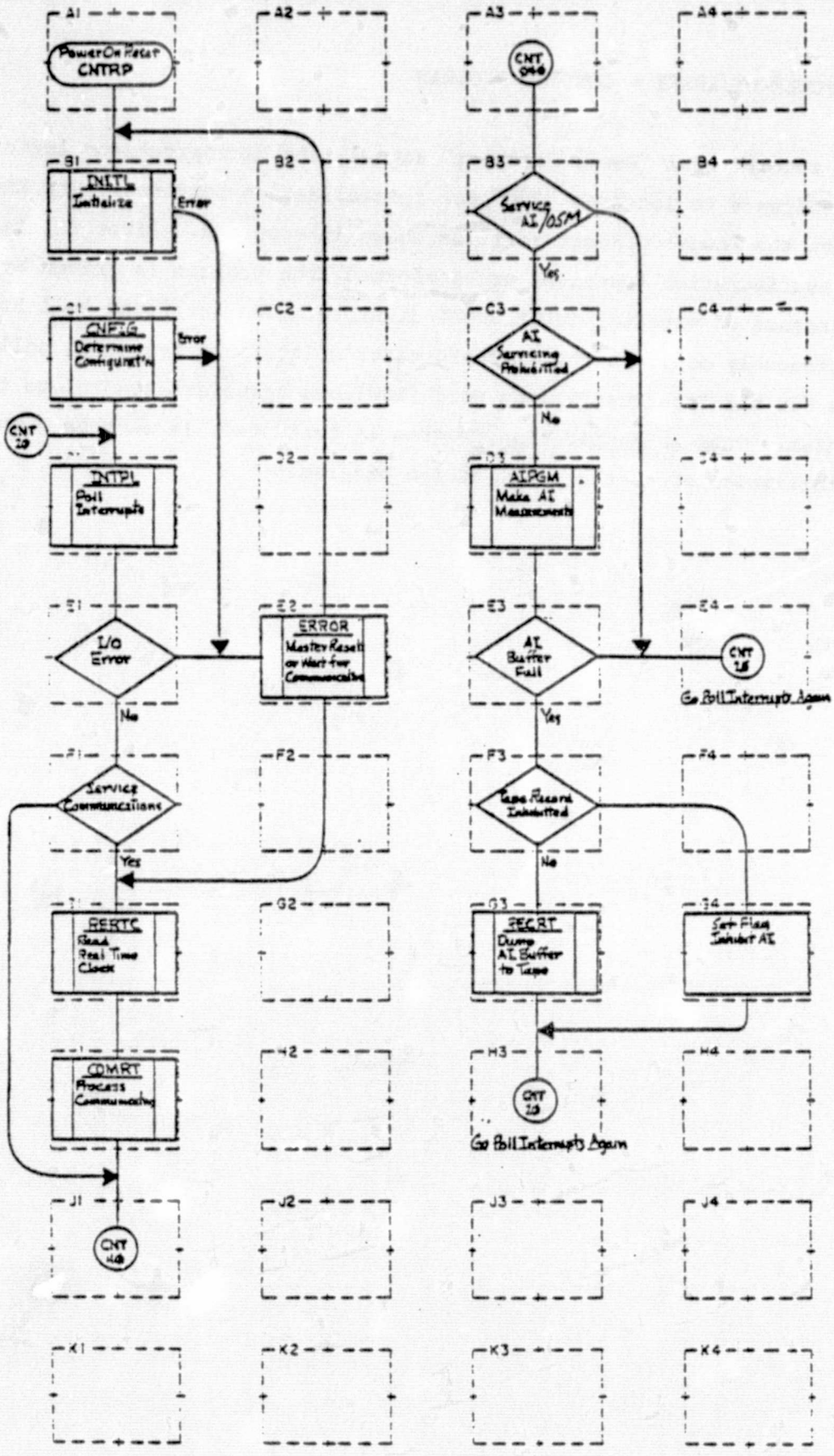


Figure 2. Control Program Overview

3. INITIALIZATION

The initialization program is called upon occurrence of a Microprocessor Power-On/Reset and performs the function of:

(1) Initialization of Random-Access Memory (RAM) to "zero"
(2) Initialize Hardware Status (Tape)
(3) Set Station-Address Field to proper value
(4) Test for Hardware Error Conditions (Tape)
(5) Exit to "Configuration" Program for further initialization if no errors exist
(6) Exit to "Error" Program is errors exist

Functional flow diagram of initialization is shown in Figure 3.

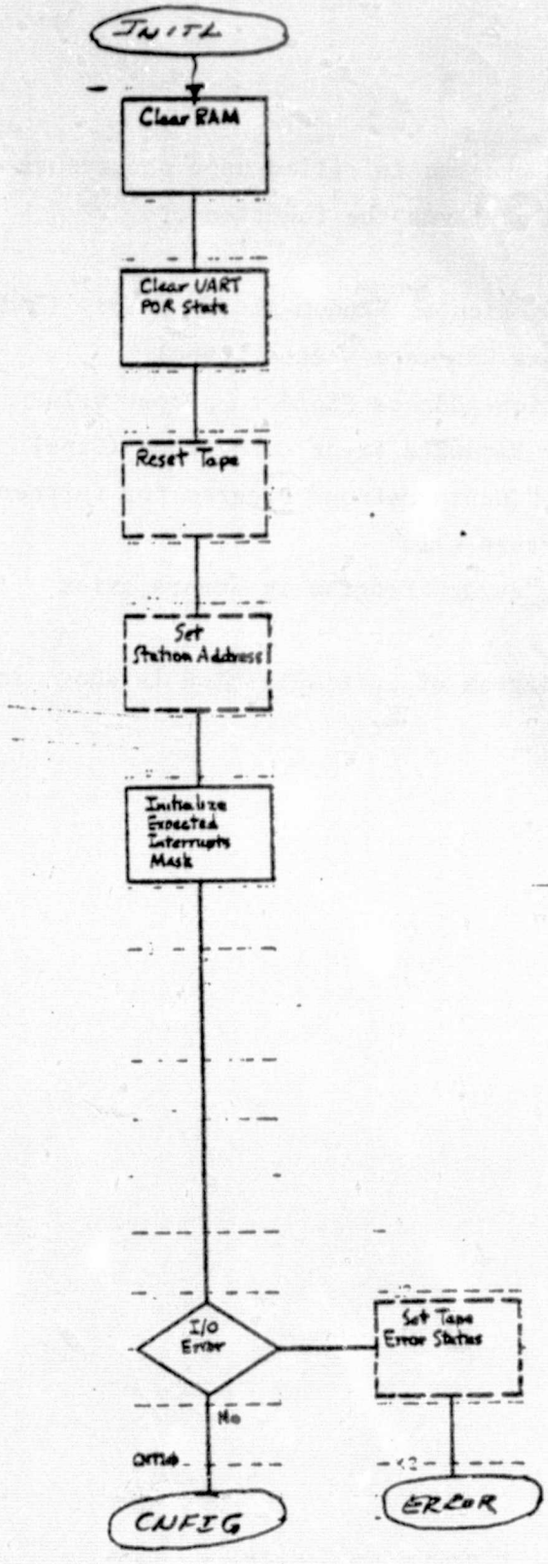


Figure 3. Initialization (INITL)

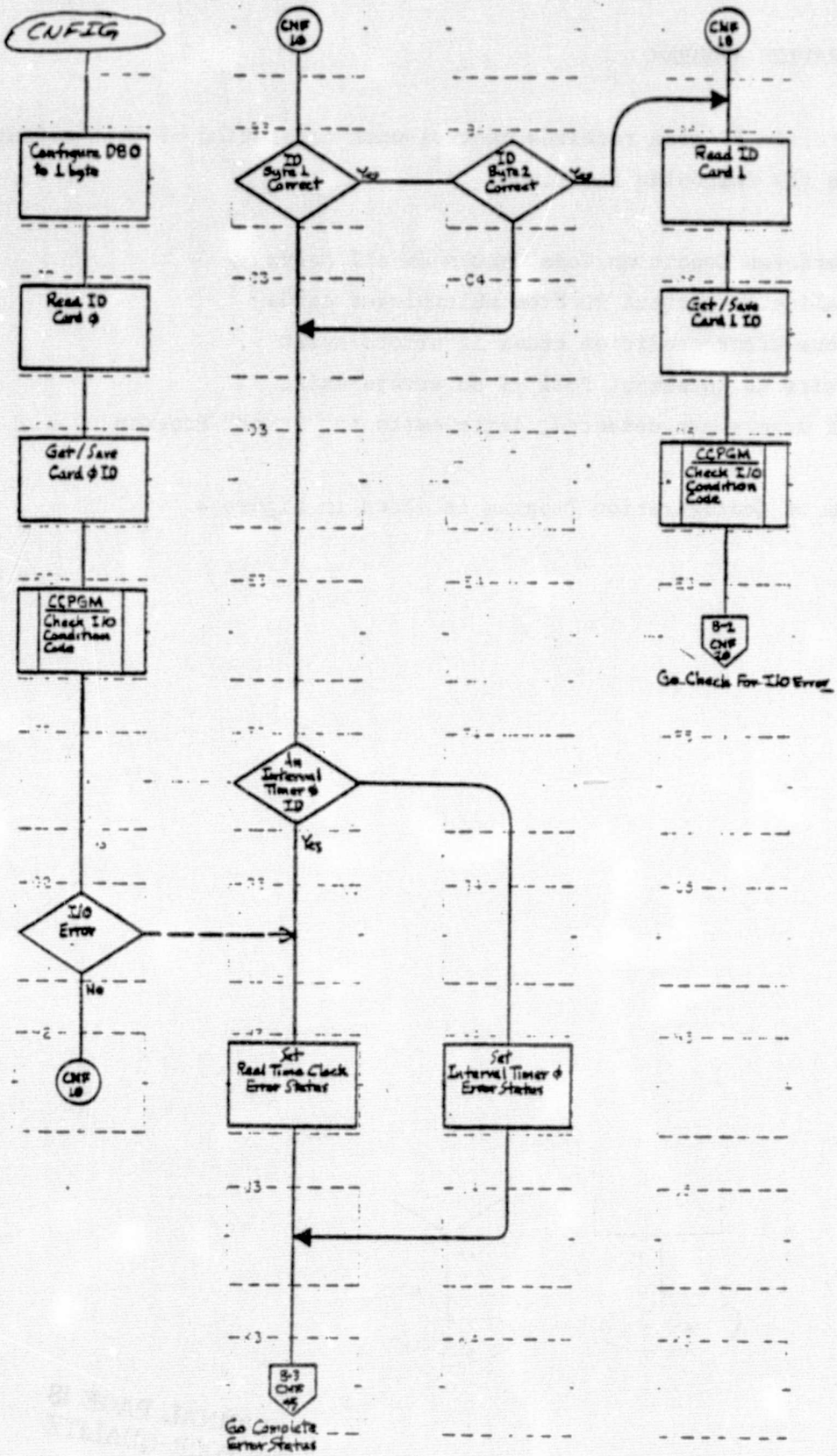


Figure 4. Configuration Procedure (Page 1 of 5)

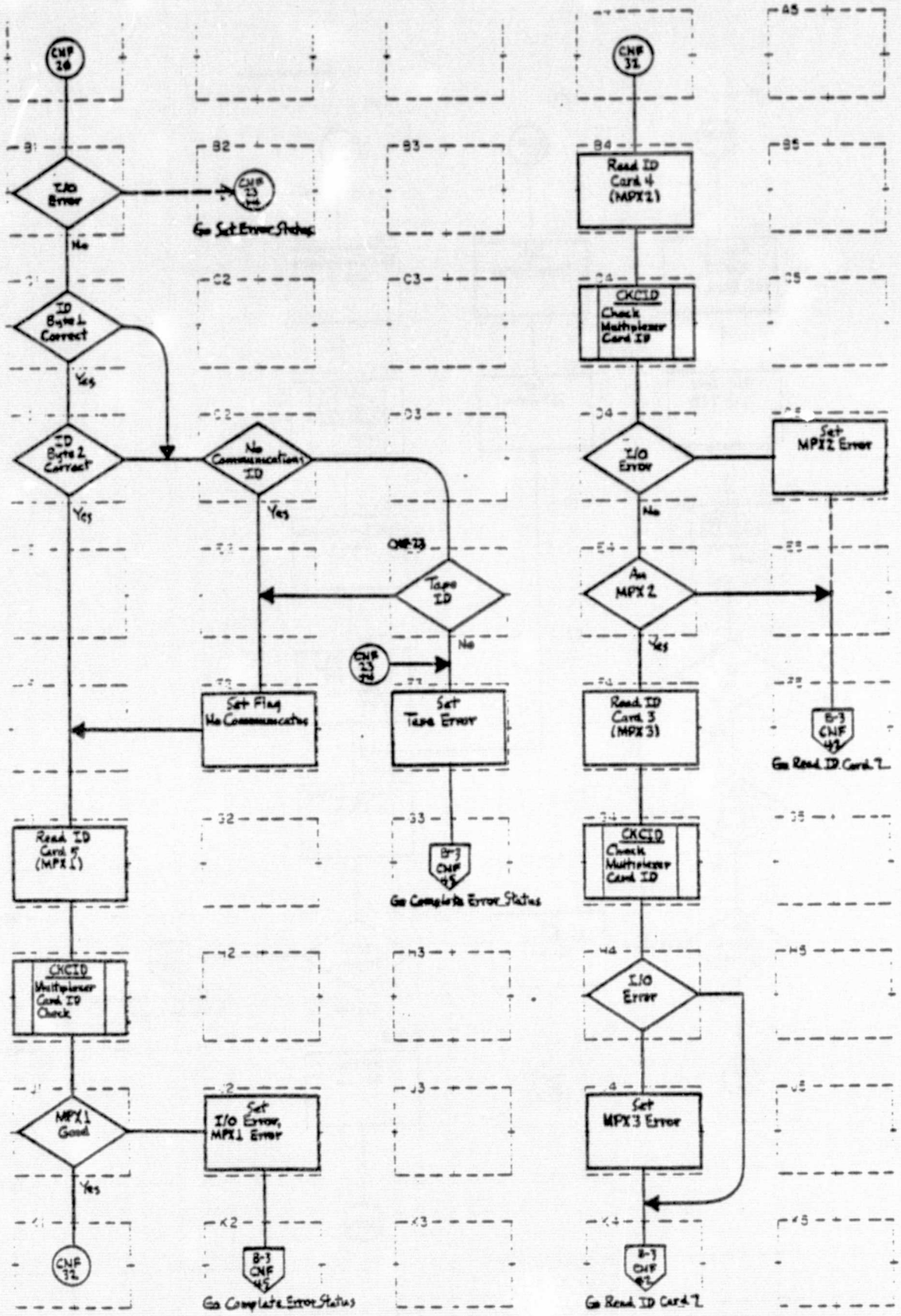


Figure 4. Configuration Procedure (Page 2 of 5)

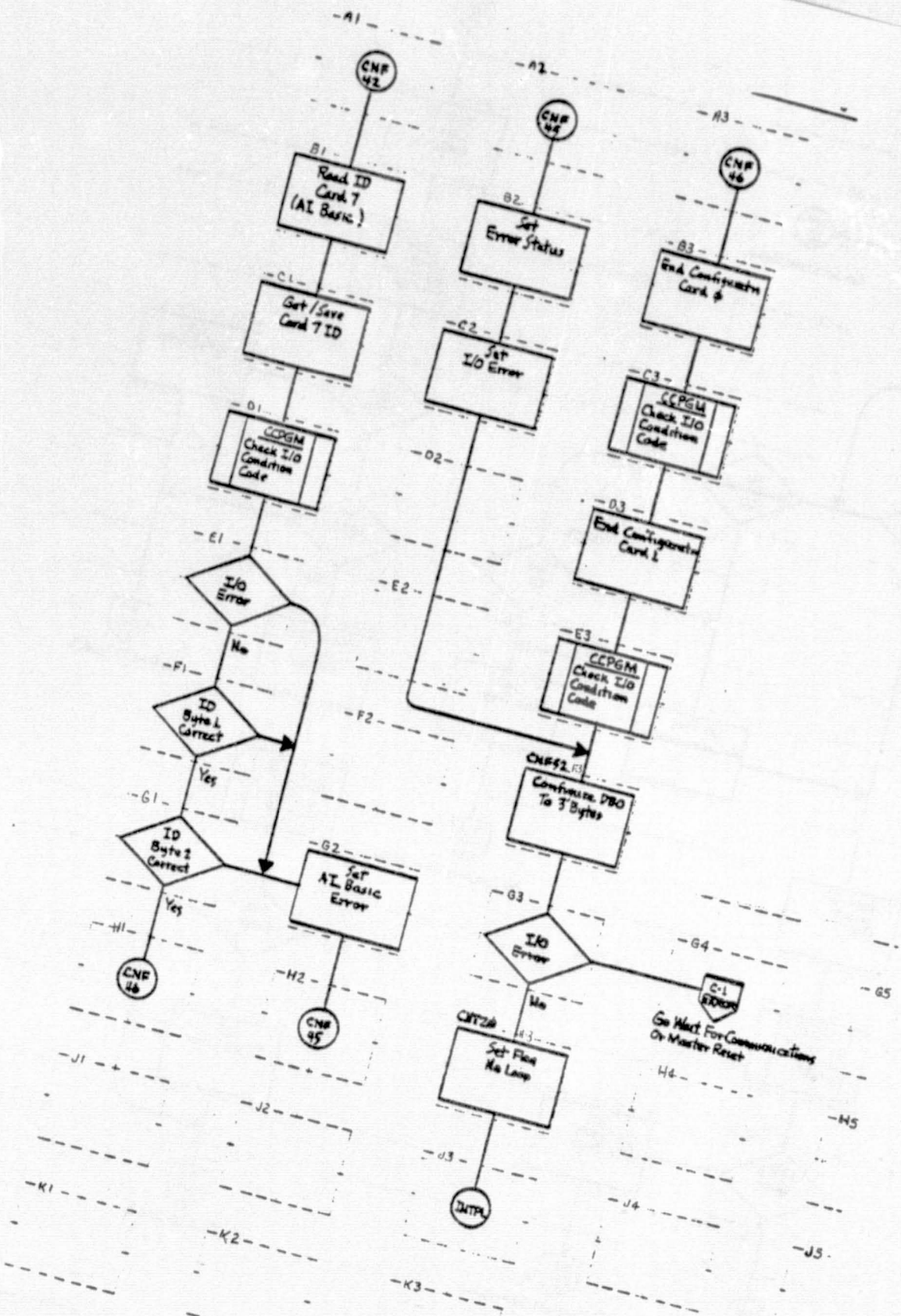


Figure 4. Configuration Procedure (Page 3 of 5)

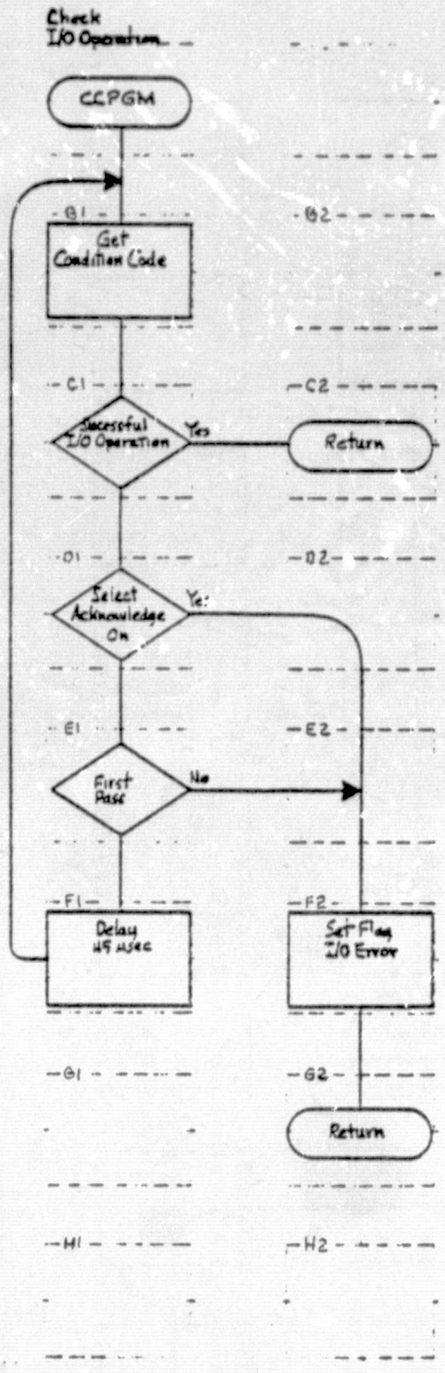


Figure 4. Configuration Procedure (Page 4 of 5)

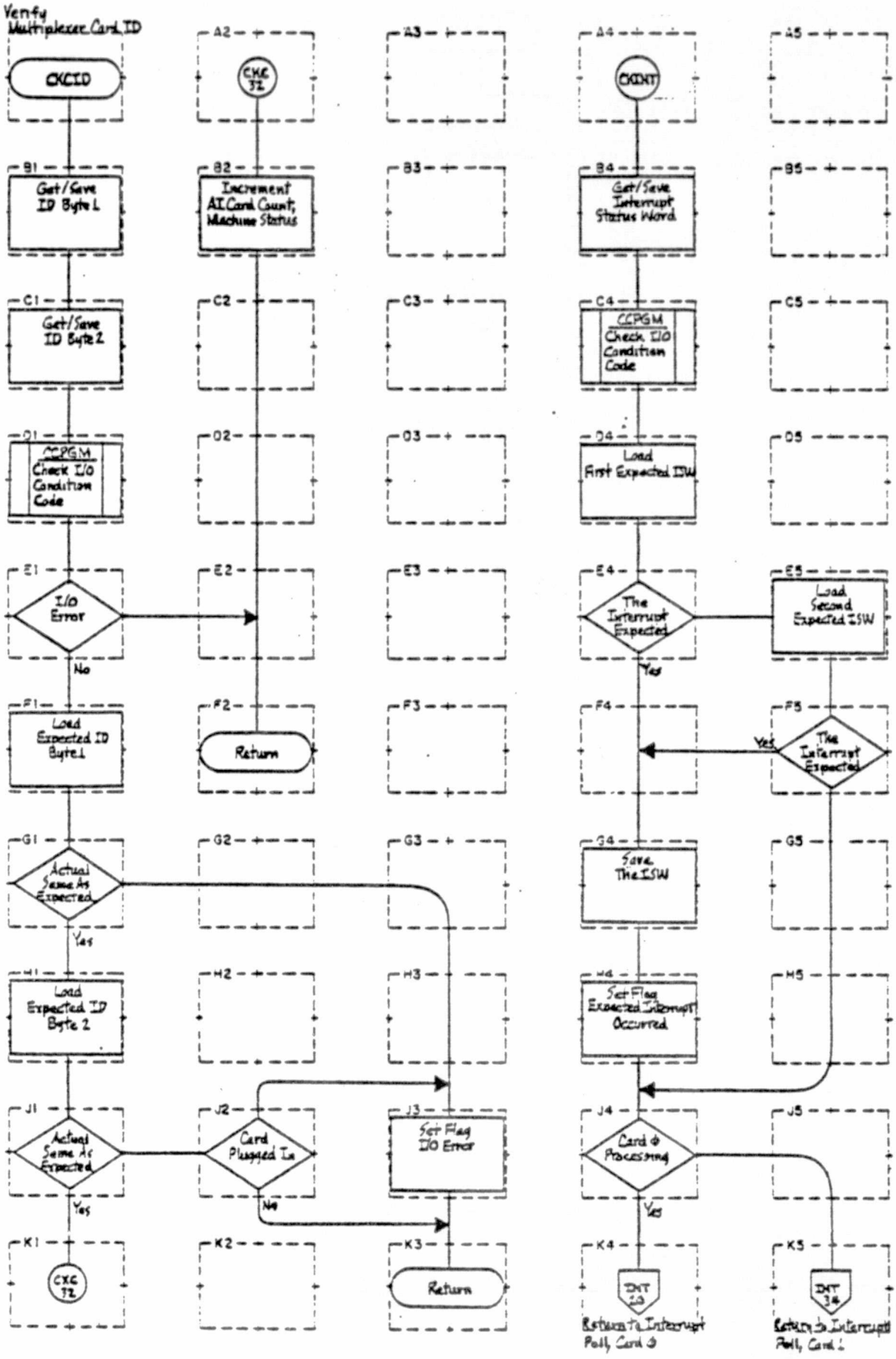


Figure 4. Configuration Procedure (Page 5 of 5)

5. INTERRUPT POLL PROGRAM

The Interrupt Poll Program reads the interrupt register and interrupt status word and determines the requested application program to be executed. Logic control is passed to the appropriate program. If errors are detected, error condition codes are set, and control is passed to the "Error" Program. Upon completion of requested applications, control returns to Interrupt Poll Program to continue checking for external interrupt requests.

Flow diagram of the Interrupt Poll Program is shown in Figure 5.

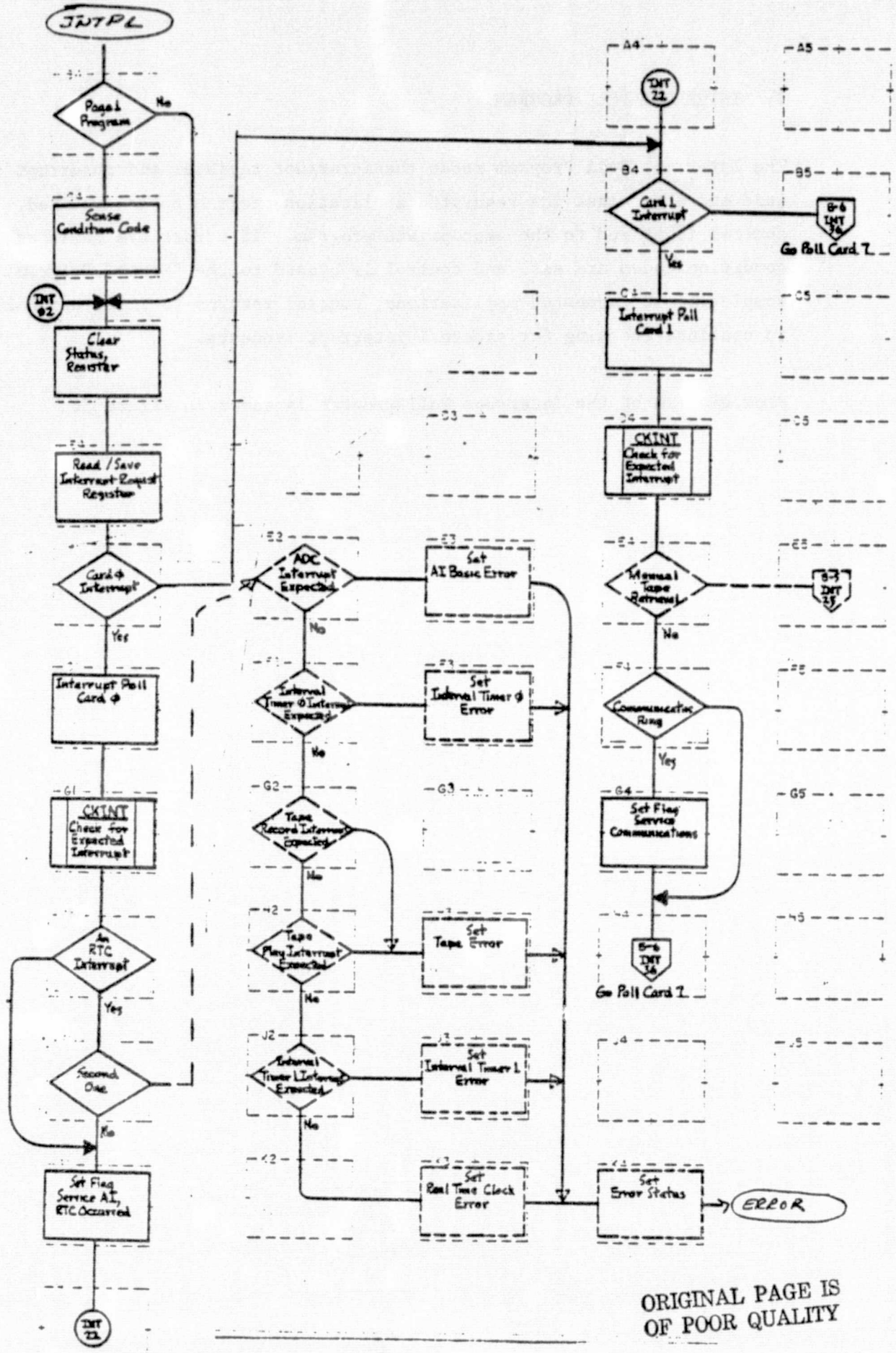


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Figure 5. Interrupt Poll Program (Page 1 of 3)

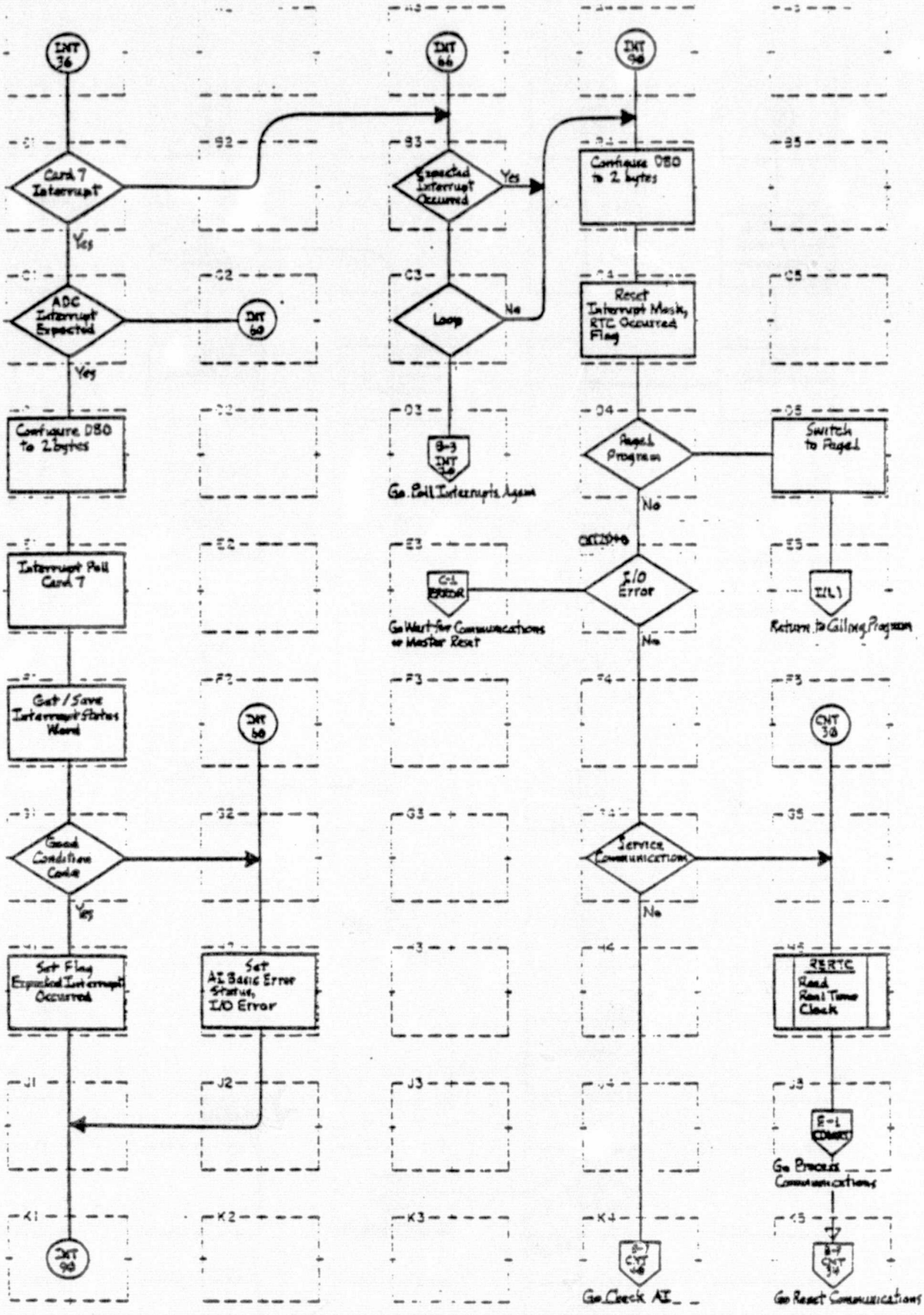

Figure 5. Interrupt Poll Program (Page 2 of 3)

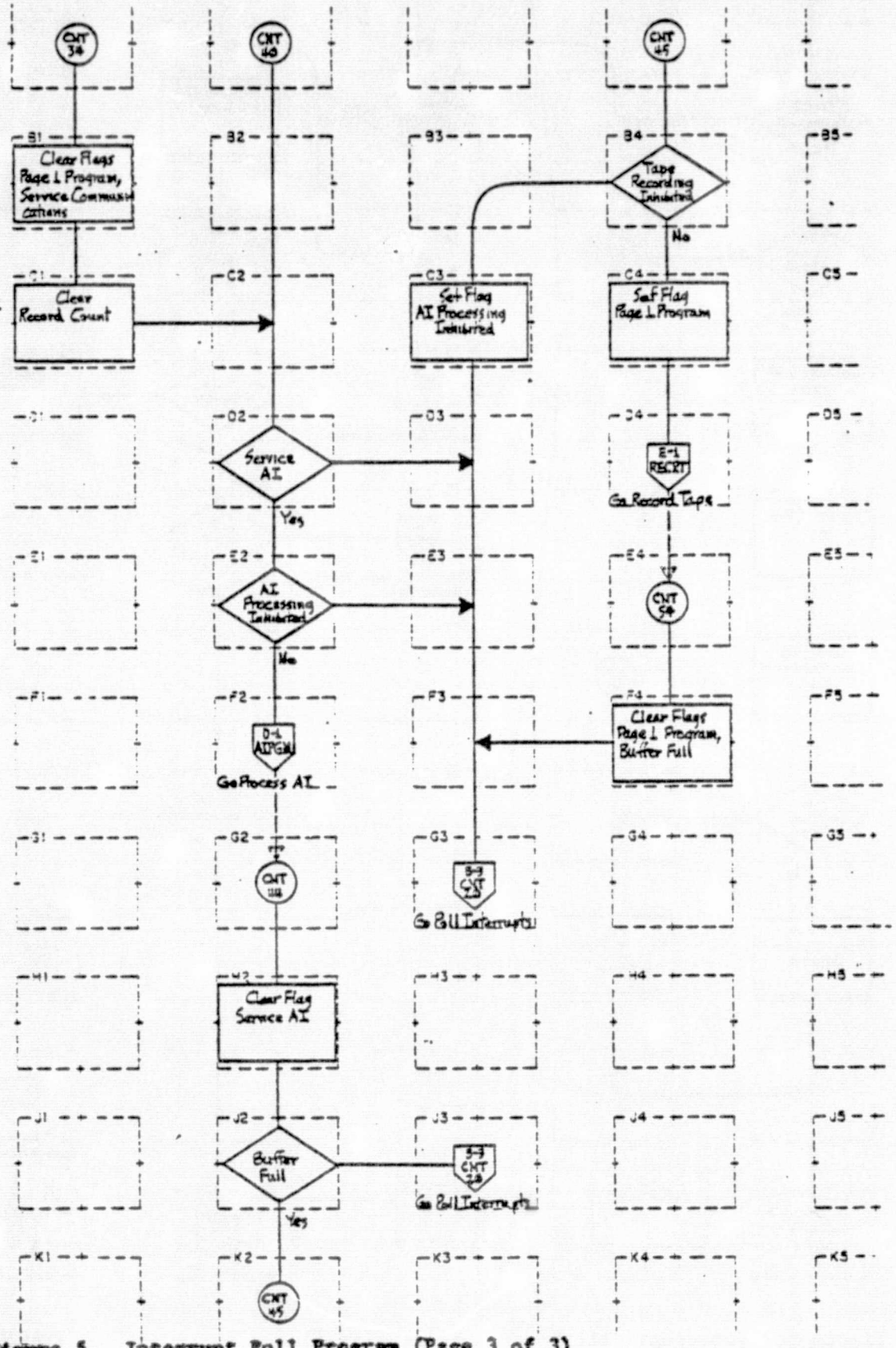

Figure 5. Interrupt Poll Program (Page 3 of 3)

6. ERROR PROCESSING (ERROR)

The Error Processing Program is entered upon determination of a SDAS hardware error. The program enters a loop awaiting a call from the S/7 for status information. Upon detection of a 'RING' from the S/7, the program passes control to the communication program for transmission of error status to S/7.

Flow diagram of ERROR Program is shown in Figure 6.

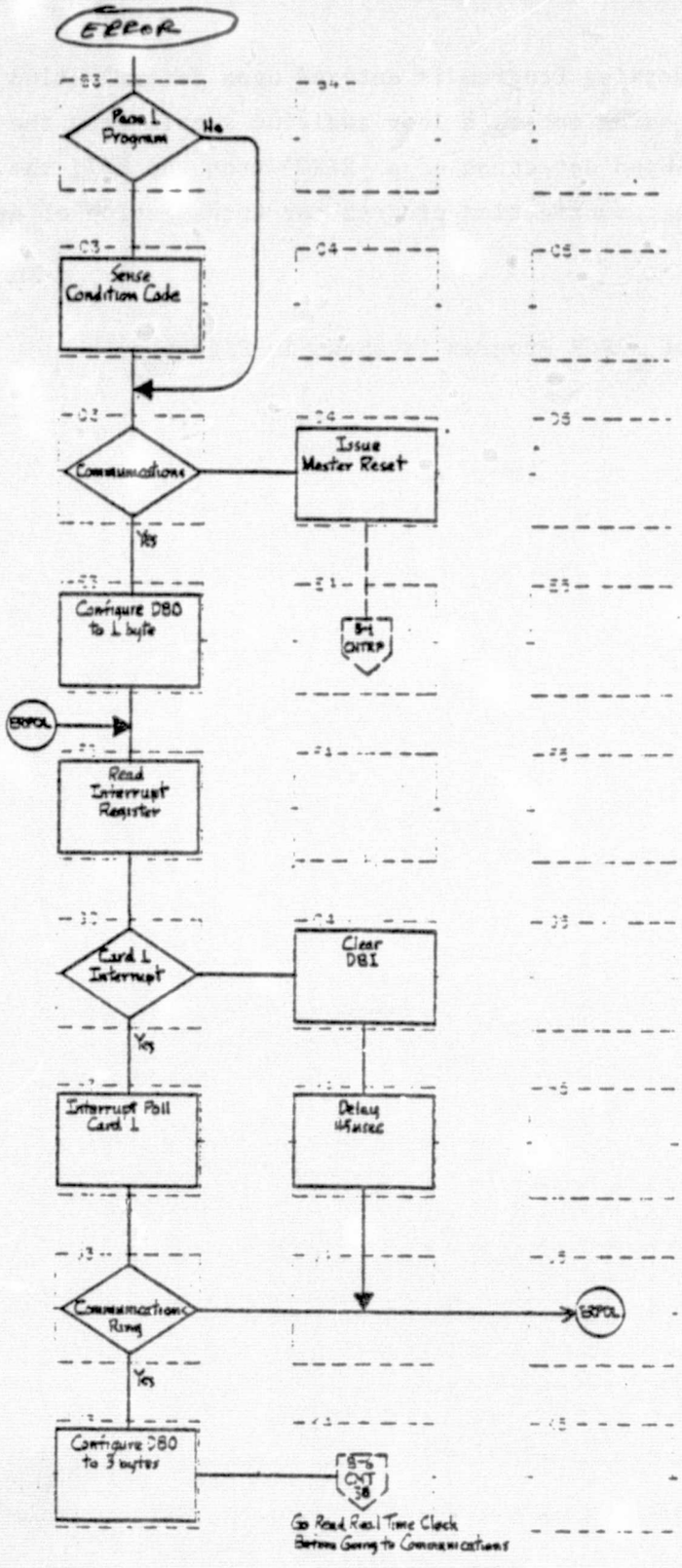

Figure 6. Error Program

7. READ REALTIME CLOCK (RERTC)

The Read Realtime Clock Program is a common subroutine used by application and control programs to provide a timekeeping capability. Because the clock can be changing during a read, two consecutive reads with identical results are required prior to storing the clock value and returning to the calling program.

8. COMMUNICATION PROGRAM (COMRT)

The communication routine handles both transmit and receive modes for the SDAS. In receive mode, SDAS will accept a command from the System/7 and check it for validity. The communication routine switches to transmit, branches to the appropriate command subroutine and transmits a reply message.

The valid commands from the S/7 to the SDAS are:

(1) Read Configuration
(2) Read Configuration plus End-of-File
(3) Disconnect
(4) Disconnect and Rewind
(5) Rewind
(6) Reinitialize
(7) Read Storage Table

A discussion of the format of the Microprogram response to these commands as well as the actions taken by the Microprogram is contained in the following paragraphs. The flow diagram for Communications Program (COMRT) is shown in Figure 7.

8.1 READ CONFIGURATION

This command will send to the System/7 the status of the SDAS. The format for this response is:

PAD/SYNC/COMMAND/SA/STATUS/RC1/RC2/T1/T2/T3/BCH/PAD

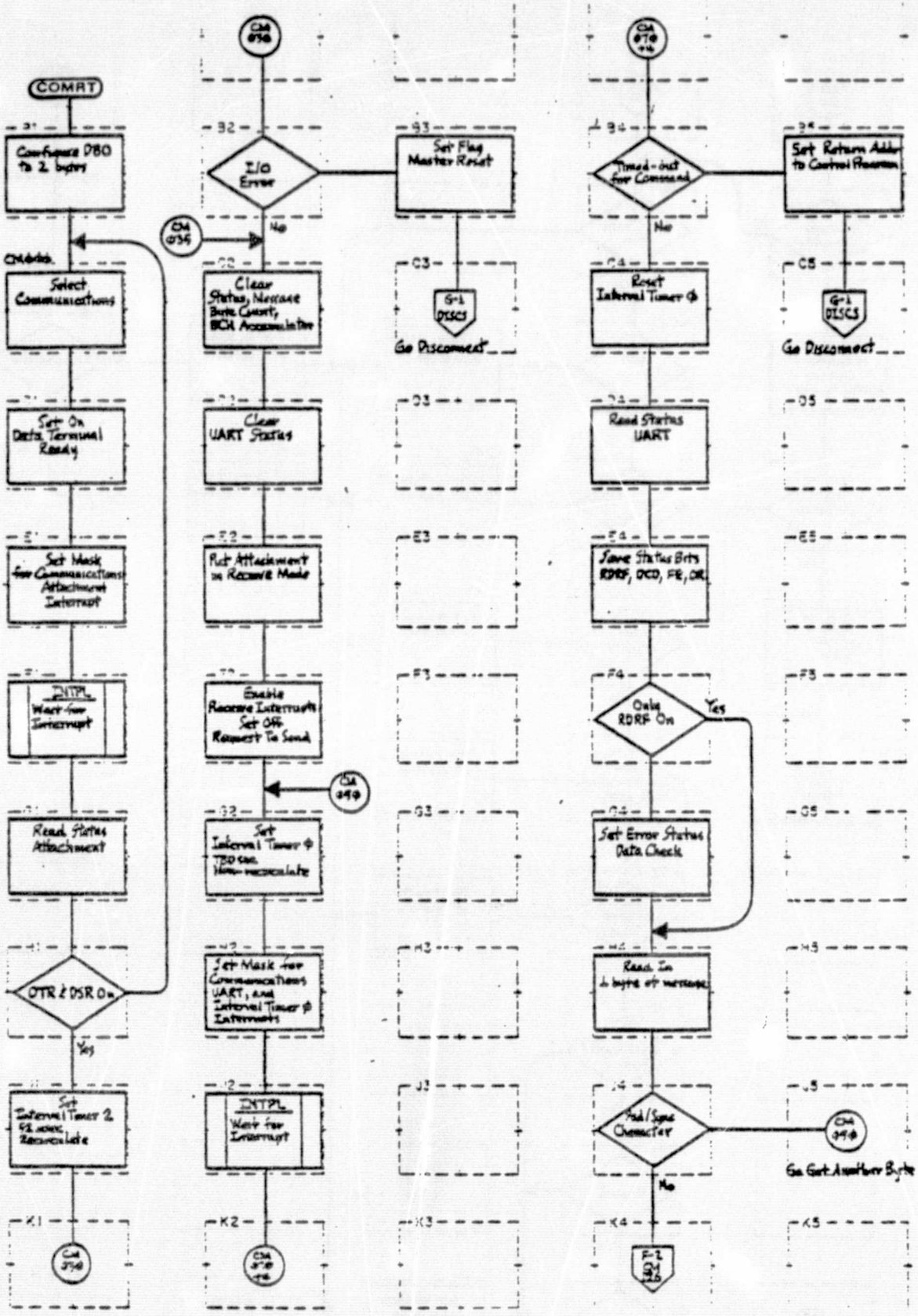

Figure 7. Communications Program (Page 1 of 12)

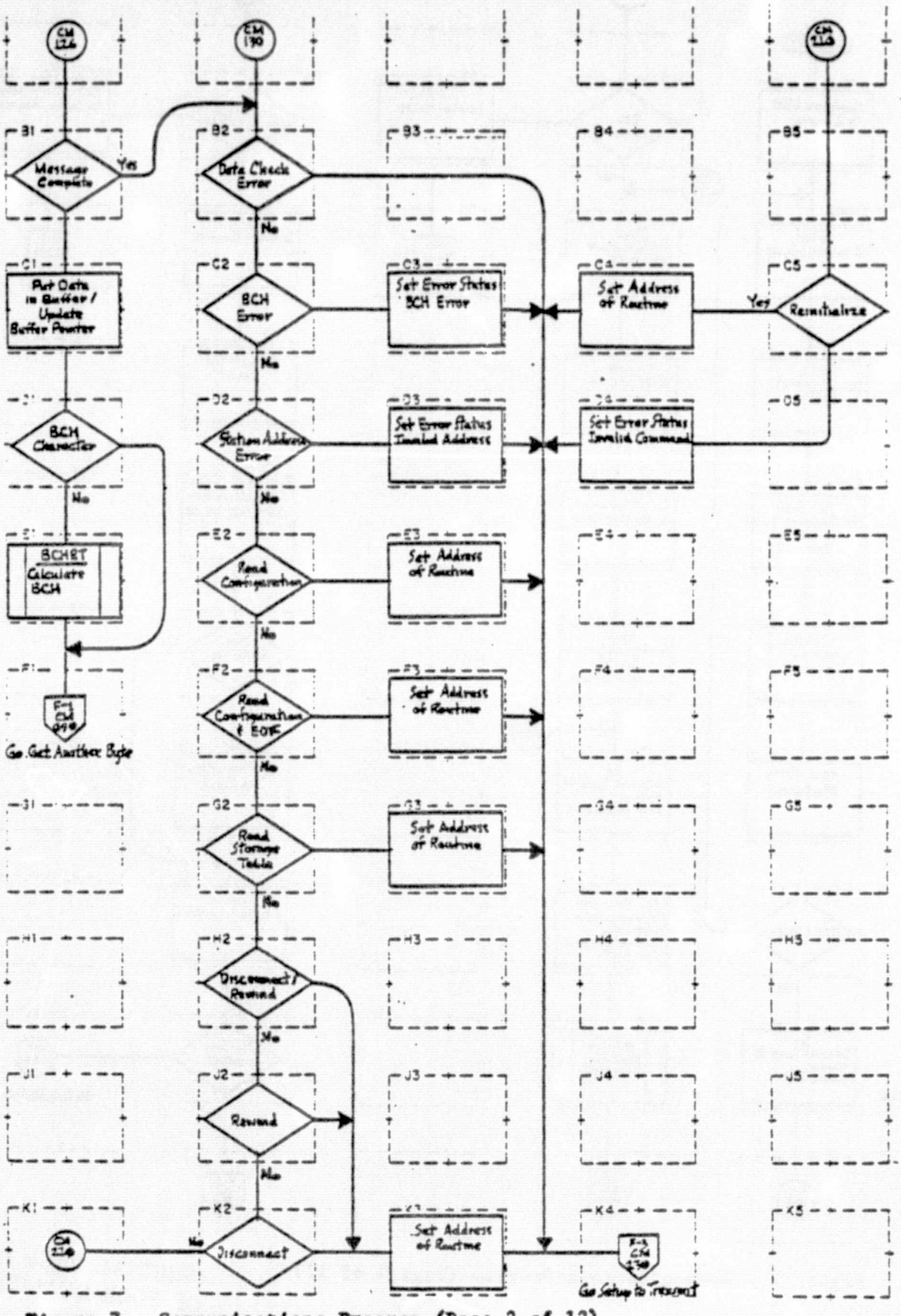

Figure 7. Communications Program (Page 2 of 12)

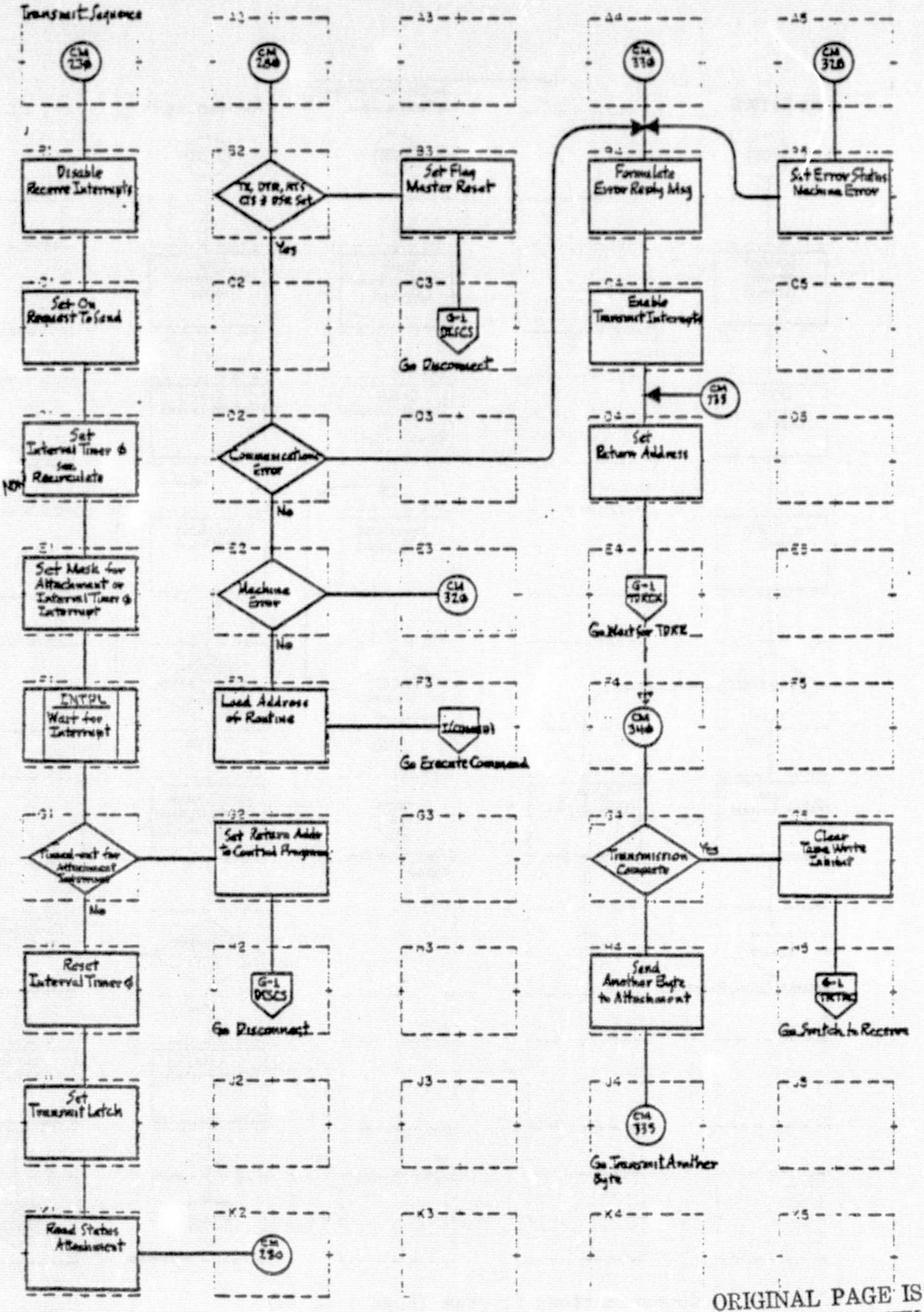

Figure 7. Communications Program (Page 3 of 12)

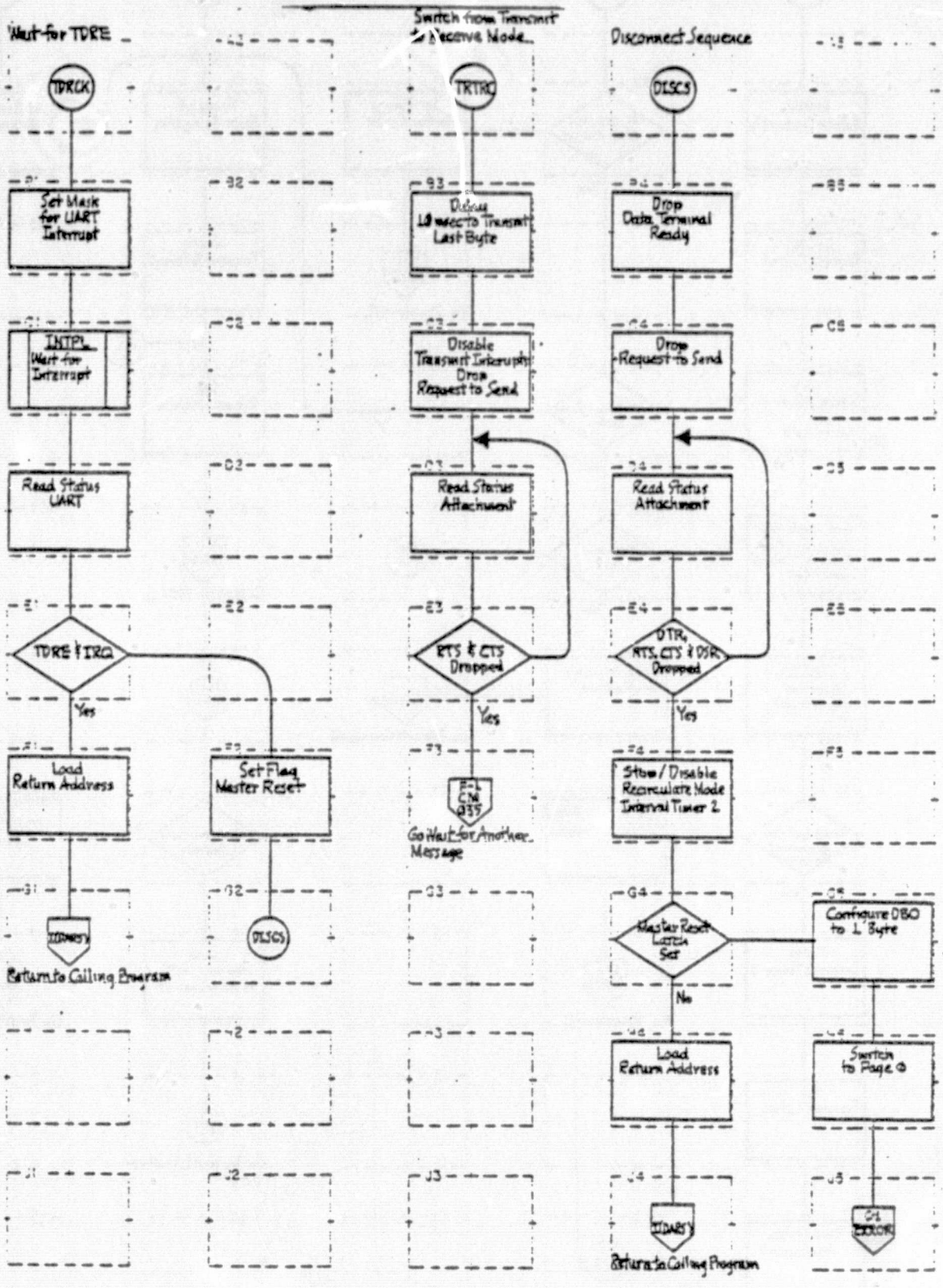

Figure 7. Communications Program (Page 4 of 12)

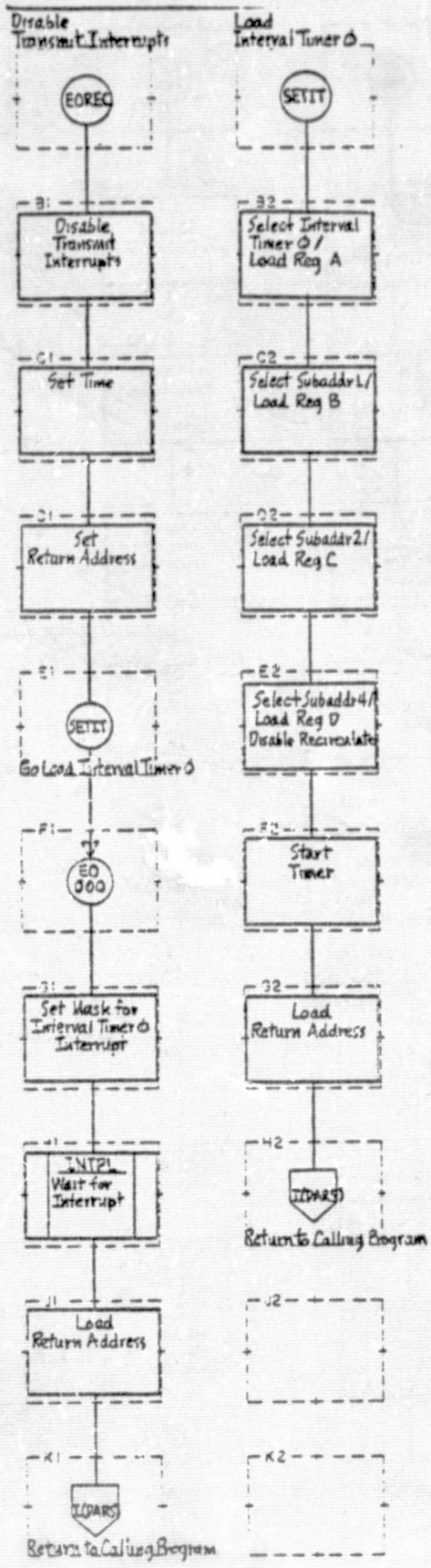

Figure 7. Communications Program (Page 5 of 12)

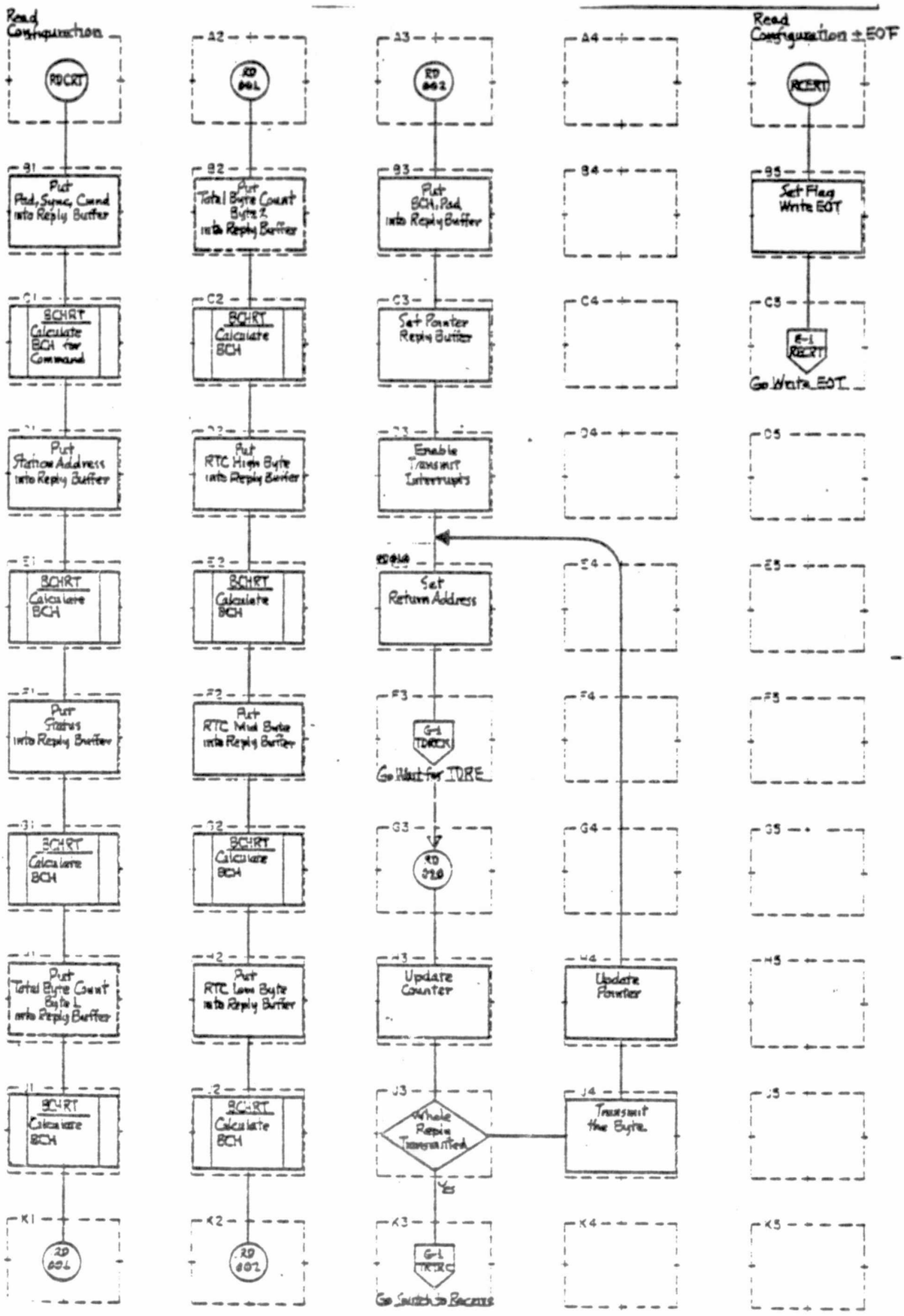

Figure 7. Communications Program (Page 6 of 12)

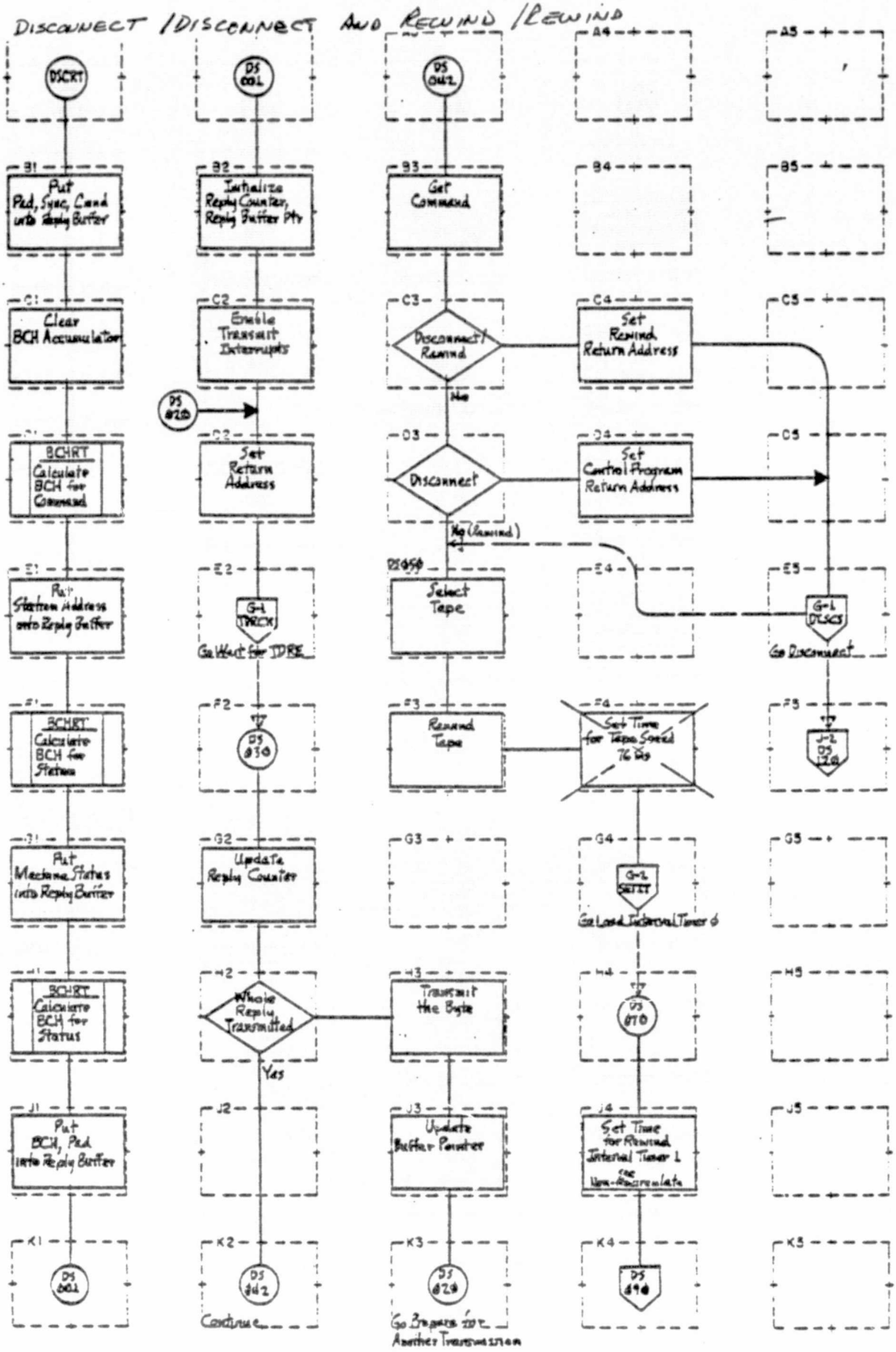

Figure 7. Communications Program (Page 7 of 12)

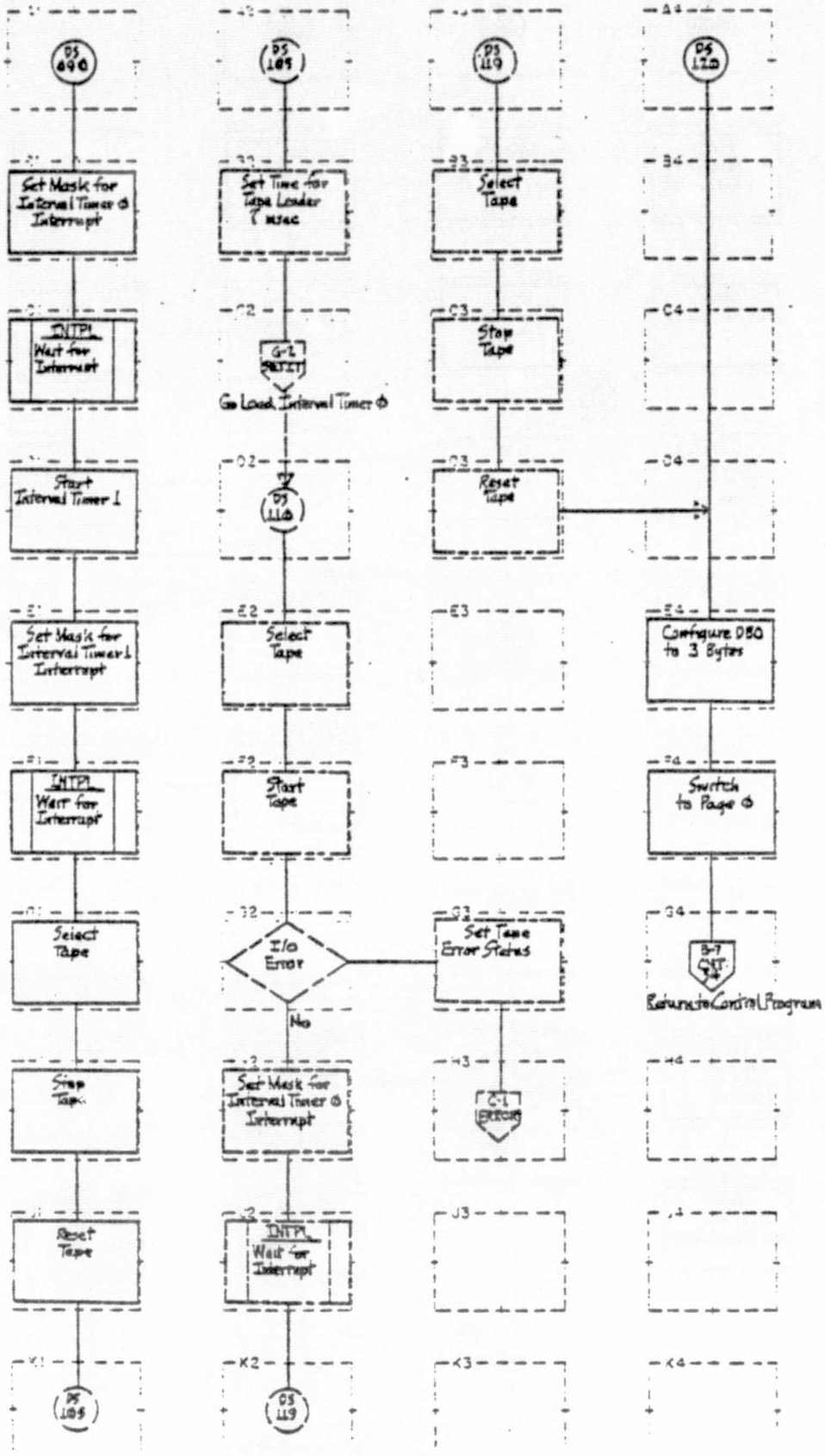

Figure 7. Communications Program (Page 8 of 12)

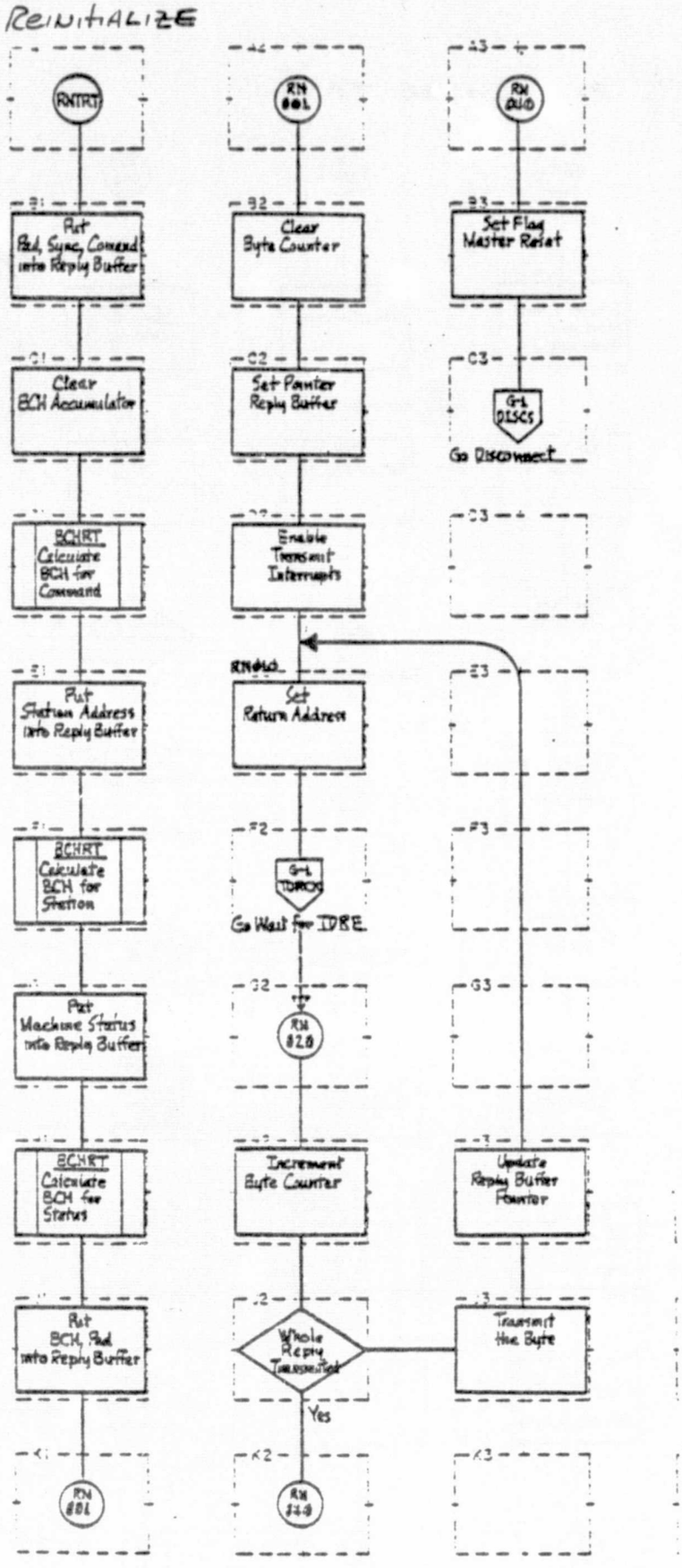

Figure 7. Communications Program (Page 9 of 12)

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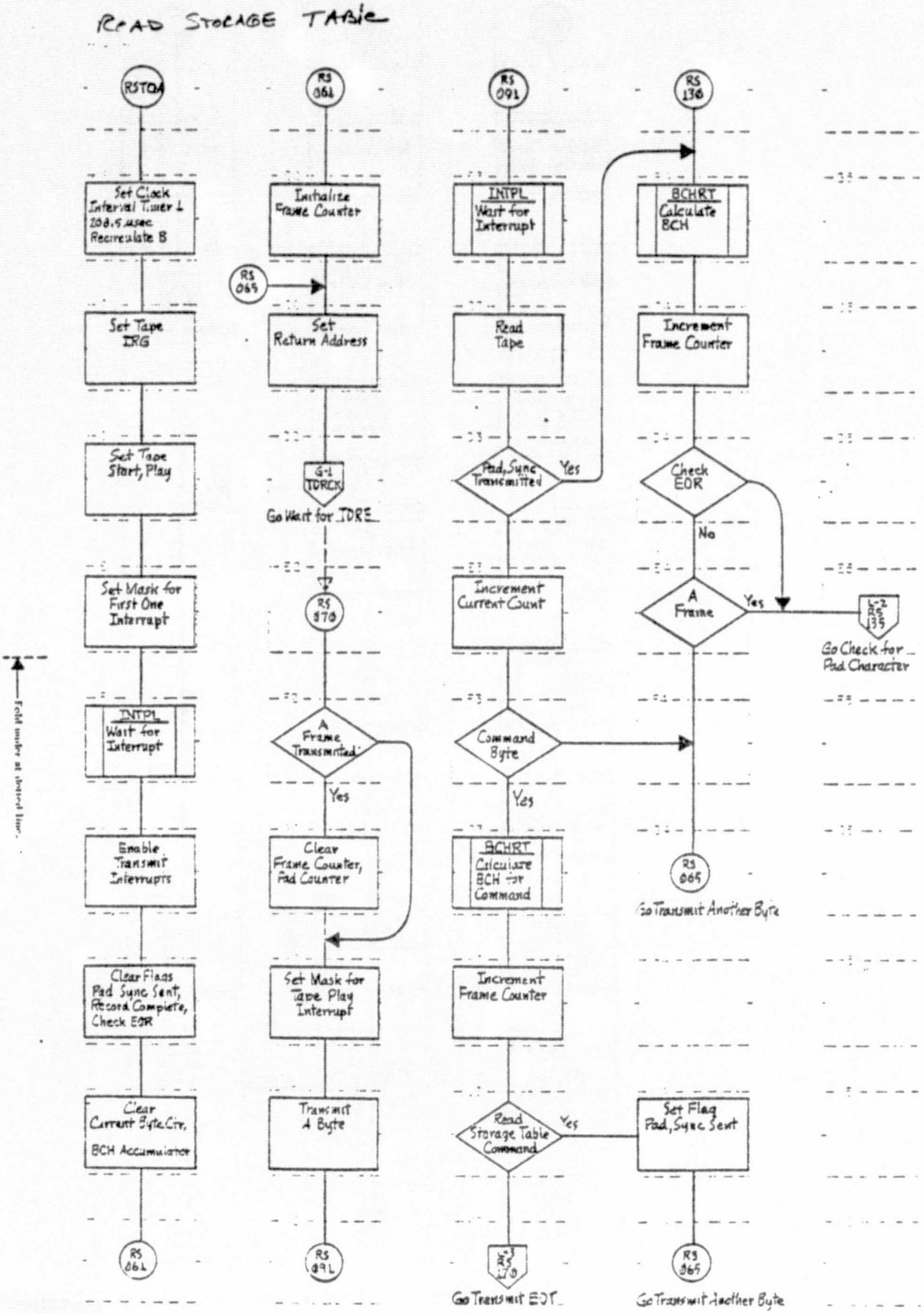

Figure 7. Communications Program (Page 10 of 12)

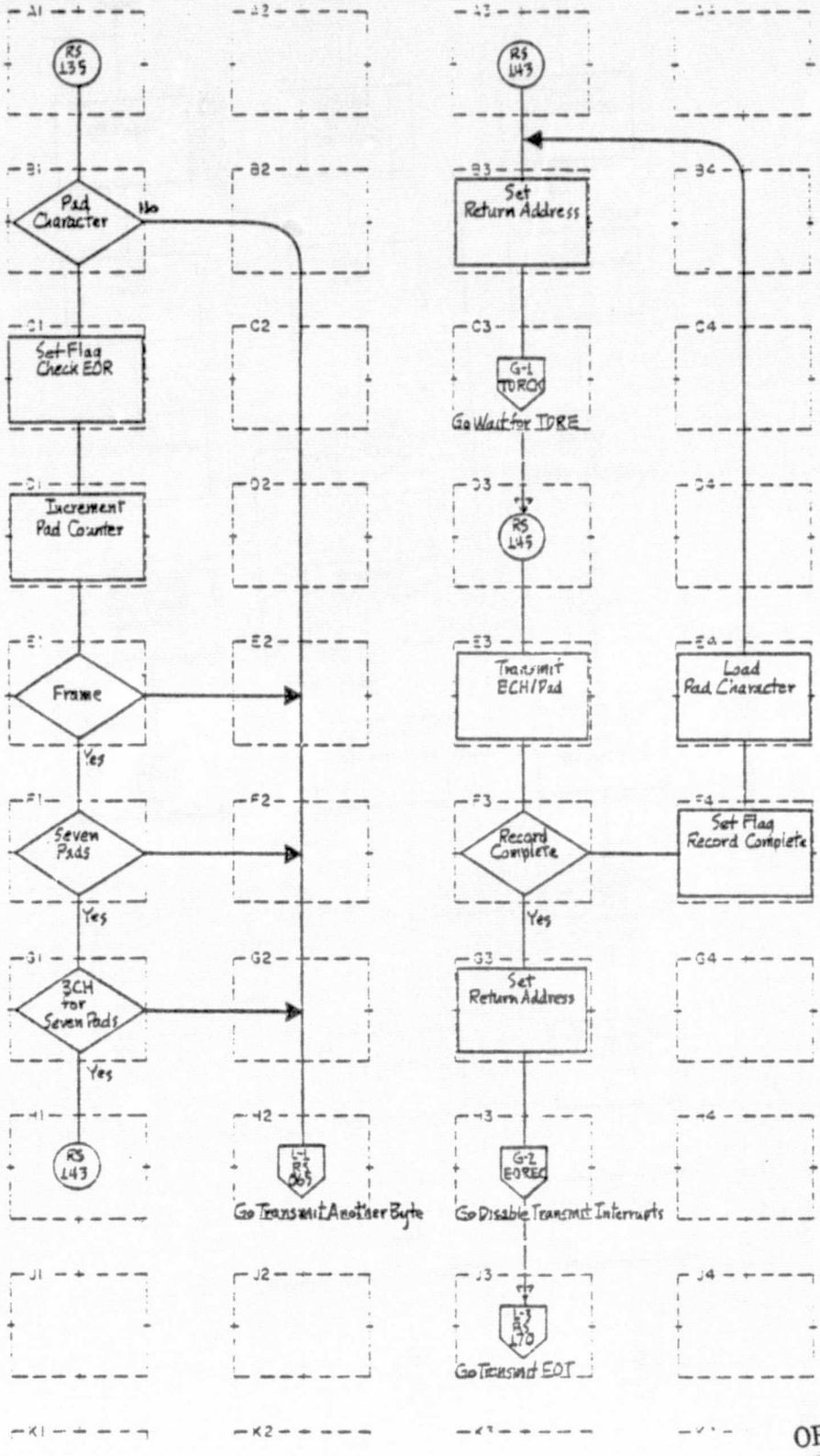

Figure 7. Communications Program (Page 11 of 12)

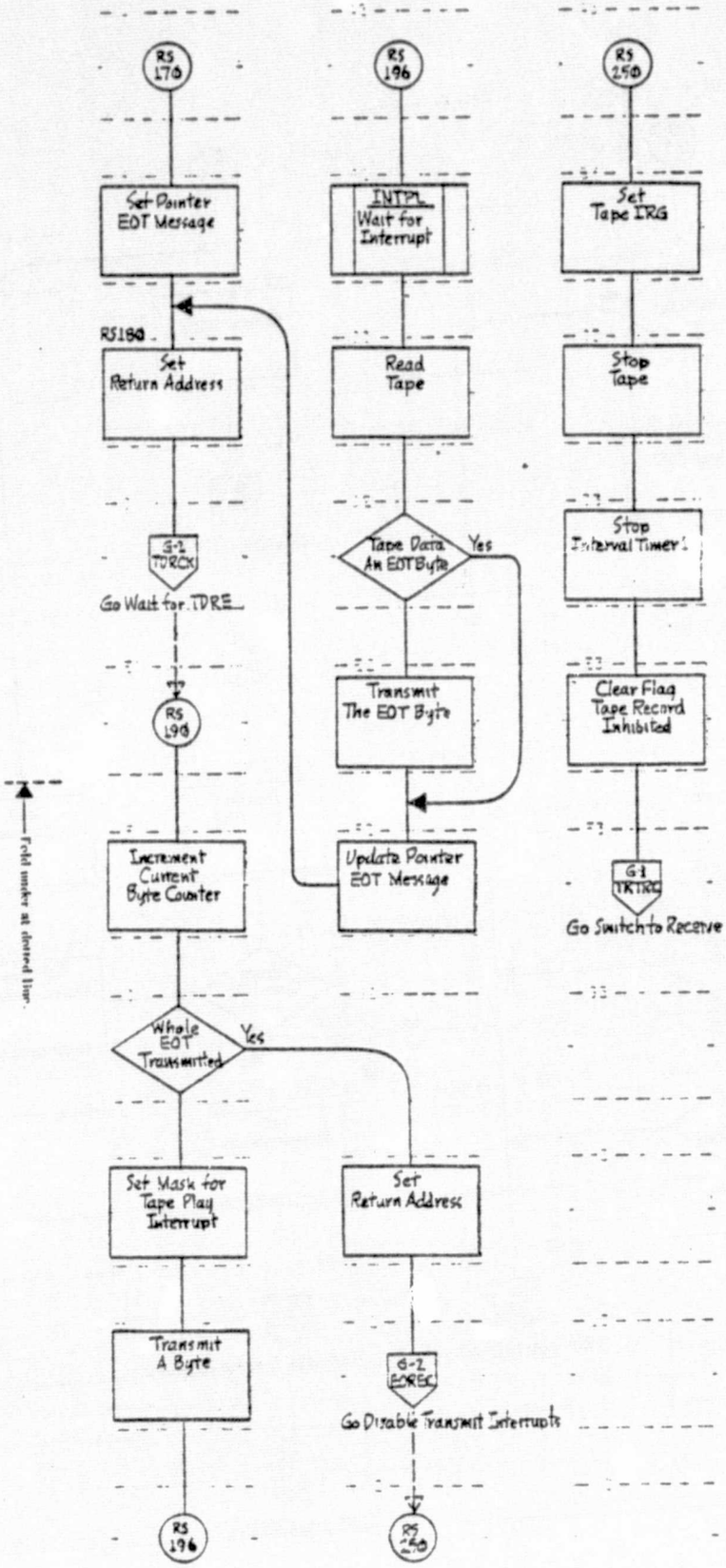

Figure 7. Communications Program (Page 12 of 12)

Where:

COMMAND	-	'2F'
SA	-	Station Address
STATUS	-	SDAS Status
RC1 and RC2	-	Record Count (total since last POR or communication)
T1, T2, and T3	-	Time Communication Started

The 1 byte status word has the following meaning;

NON-ERROR STATUS

CODE	DEVICE
05	MPX 1 exists
06	MPX 1 and 2 exists
07	MPX 1, 2, and 3 exist

ERROR STATUS - COMMAND

CODE	ERROR
90	BCH error
80	Invalid command
81	Invalid station address
84	Data set check

ERROR STATUS - MICROPROCESSOR

CODE	DEVICE ERROR
C0	MPX 1
C1	MPX 2
C2	MPX 3
C3	AI Basic
C4	Interval Timer 0
C5	Tape Control
C6	Real Timer Clock

8.2 READ CONFIGURATION + EOF

This command writes an end-of-file mark on the cassette tape by branching to the record routine, RECRT. Then a reply, similar to a Read Configuration reply, is sent to the System/7. The format for the READ CONFIGURATION + EOF reply is:

PAD/SYNC/COMMAND/SA/STATUS/RC1/RC2/T1/T2/T3/BCH/PAD

Where command is equal to 'FF'.

8.3 DISCONNECT AND REWIND

The disconnect and rewind command sends a reply to the System/7, drops DTR and RTS, and then rewinds the tape. The format for this reply is:

PAD/SYNC/COMMAND/SA/STATUS/BCH/PAD

Where command is'00'.

8.4 READ STORAGE TABLE

This command transmits the AI sensor data from cassette tape to the System/7. More than 1 record can be sent with this command. Each record has the following format:

PAD/SYNC/EO COMMAND/SA/STATUS/RC1/RC2/T1/T2/T3/BCH/ 8 BYTES OF DATA/BCH/---/
8 BYTES OF DATA/BCH/8 PAD CHARACTERS/BCH/BCH/PAD

The last record on the tape is called an end-of-file mark and has the following fixed format:

FF/6C/E400/00/00/0B/FF/FF/FF/68/FF

Once this record has been transmitted to the System/7, the tape will be stopped and the SDAS will switch from transmit to receive mode.

8.5 REINITIALIZE

This command results in a master reset of the Microprocessor. The format for this command reply is:

PAD/SYNC/COMMAND/SA/STATUS/BCH/PAD

Where command equals 'F'.

8.6 DISCONNECT

This command results in a normal reply to the S/7 and disconnect from communication. The format for the reply is:

PAD/SYNC/COMMAND(55)/SA/STATUS/BCH/PAD

8.8 READ CONFIGURATION

This command will result in a read of the Real Time Clock and a reply message of the following format:

PAD/SYNC/COMMAND(2F)/SA/STATUS/RC1/RC2/T1/T2/T3/BCH/PAD

NOTES

1. To execute the communication routine the following devices must be working properly: interval timer 0, the tape attachment, the communication UART and the communication attachment.

2. After the Read Configuration, Read Configuration + EOF or Read Storage Table Command, the SDAS switches back into receive mode and expects another command from the System/7. The SDAS allows 30 seconds for the System/7 to respond. If no response occurs, the SDAS will disconnect.

3. If the System/7 wishes to check the status only of the SDAS, it should send a read configuration command, wait for reply, and then hang up. The SDAS will also hang up, and then return to the control program without inhibiting tape write or resetting the real time clock.

9. ANALOG INPUT PROCESSING (AIPGM)

The Analog Input Processing Program uses a site-dependent table to read and store sensor readings through the SDAS ADC and multiplexer cards. Scan of the analog inputs is controlled through an interrupt from the real time clock (baseline scan interval is 1.3 minutes). The program uses the AI table for determination of input range (0 mv - 100 mv or 0 v - 5 v), length of input (8 bits or 10 bits), and asynchronous sampling requirements. All multiplexer channels valid for the SDAS are sampled and ADC offset computed during each scan. The real time clock is read before each scan is taken, and the time and scan data are formatted and placed into the output buffer. A BCH character is computed and stored with each group of 8 bytes.

Asynchronous sampling of 10 input parameters is provided. Upon occurrence of the real time clock interrupt (every 32 seconds), the AI program is entered, and the 10 inputs are read and summed. When the selected baseline scan interval (5, 15, or 30 minutes) occurs, the summed values are placed into the RAM Buffer to be written to tape when the Buffer becomes full.

Upon filing buffer, indicator is set to write buffer to tape. Actual writing performed by tape program.

Flow diagram of Analog Input Processing (AIPGM) is shown in Figure 8.

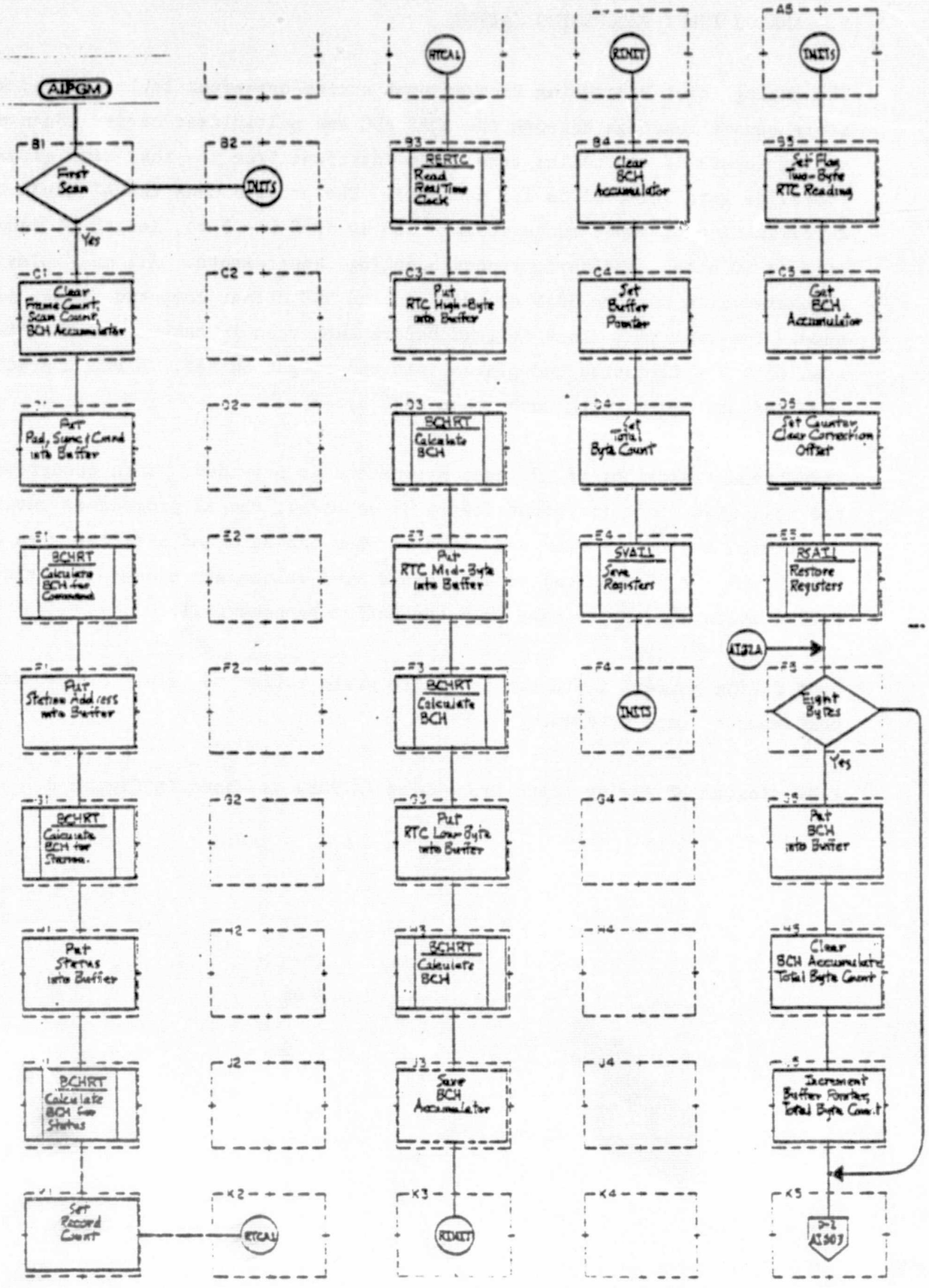

Figure 8. Analog Input Processing (Page 1 of 6)

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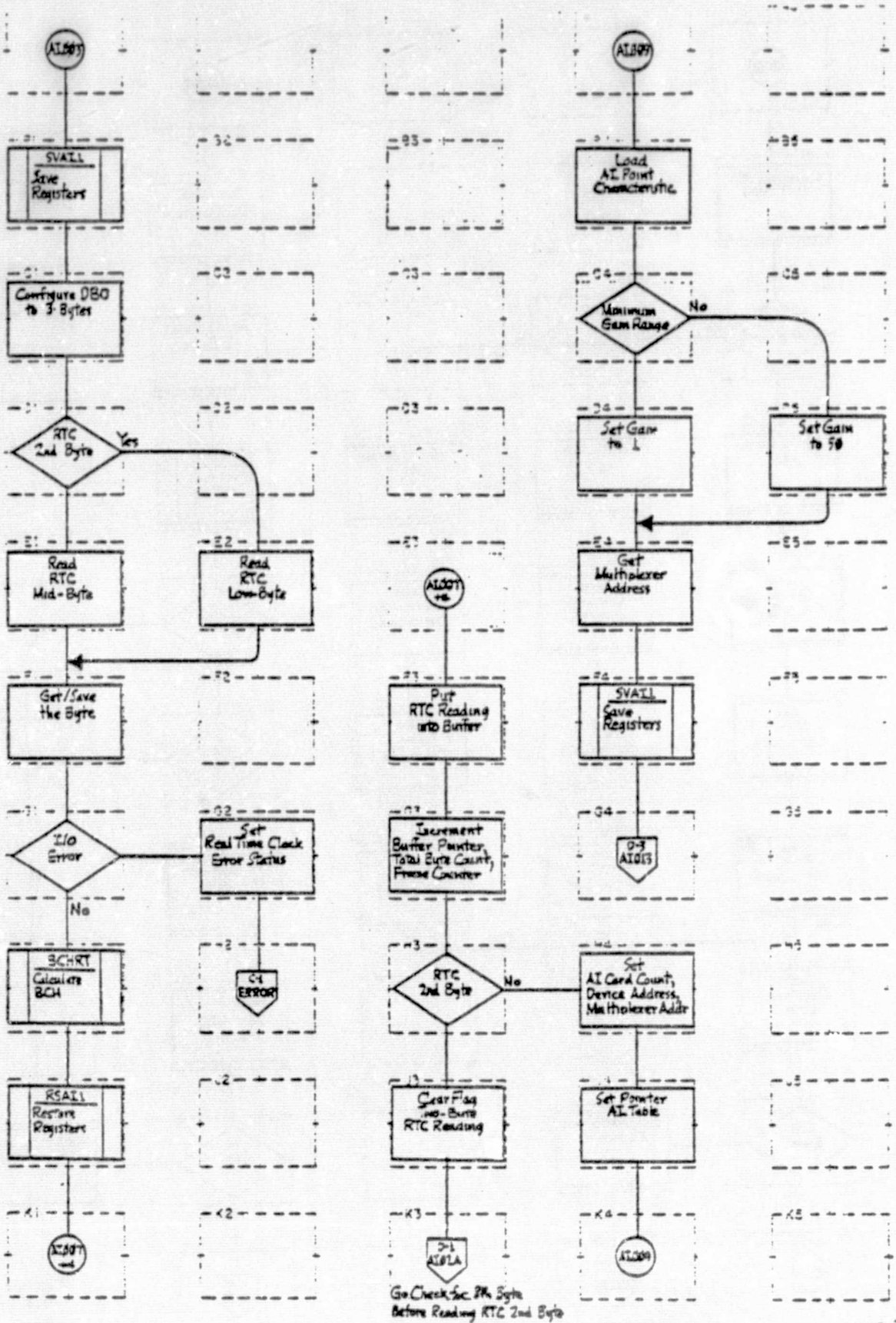

Figure 8. Analog Input Processing (Page 2 of 6)

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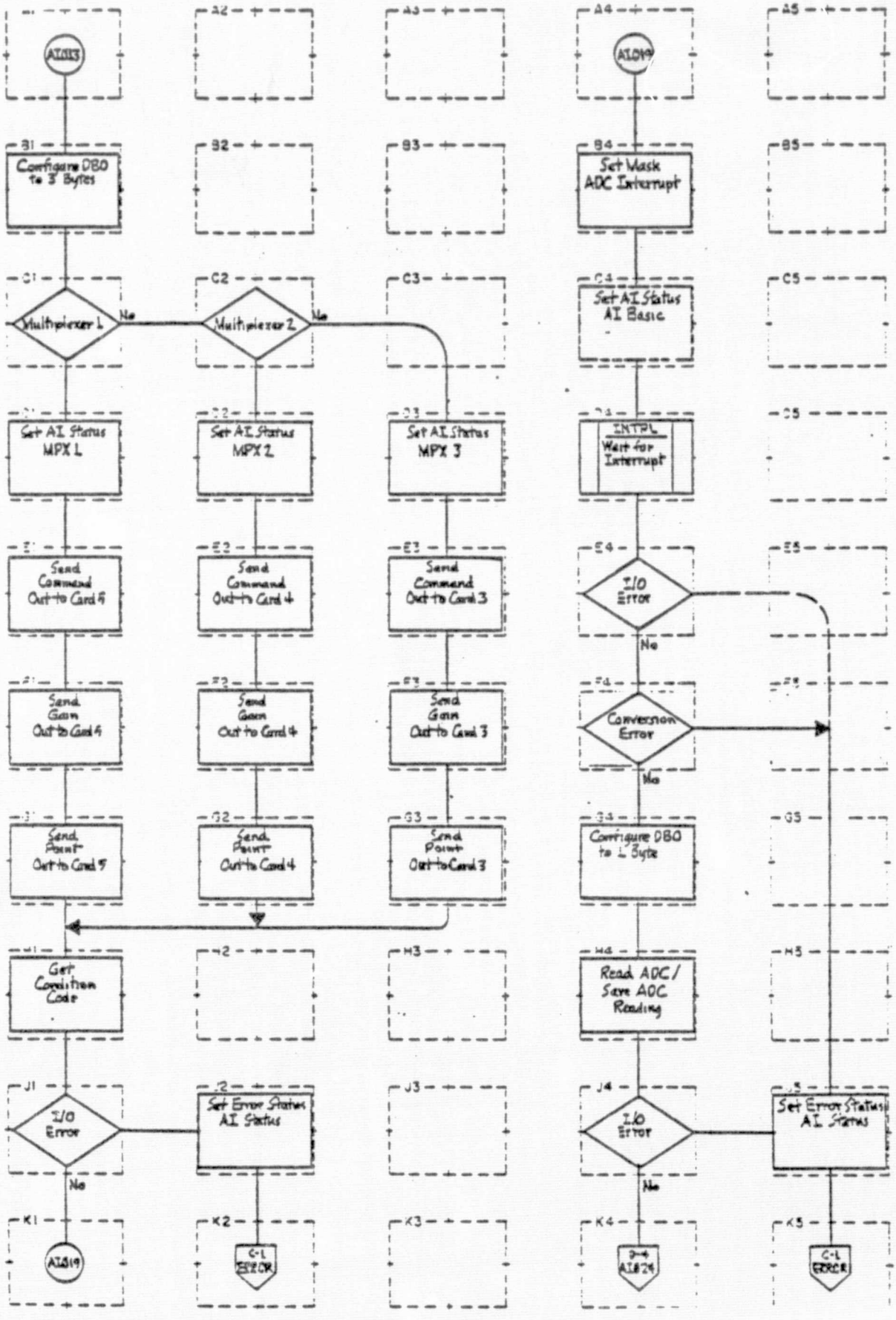

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Figure 8. Analog Input Processing (Page 3 of 6)

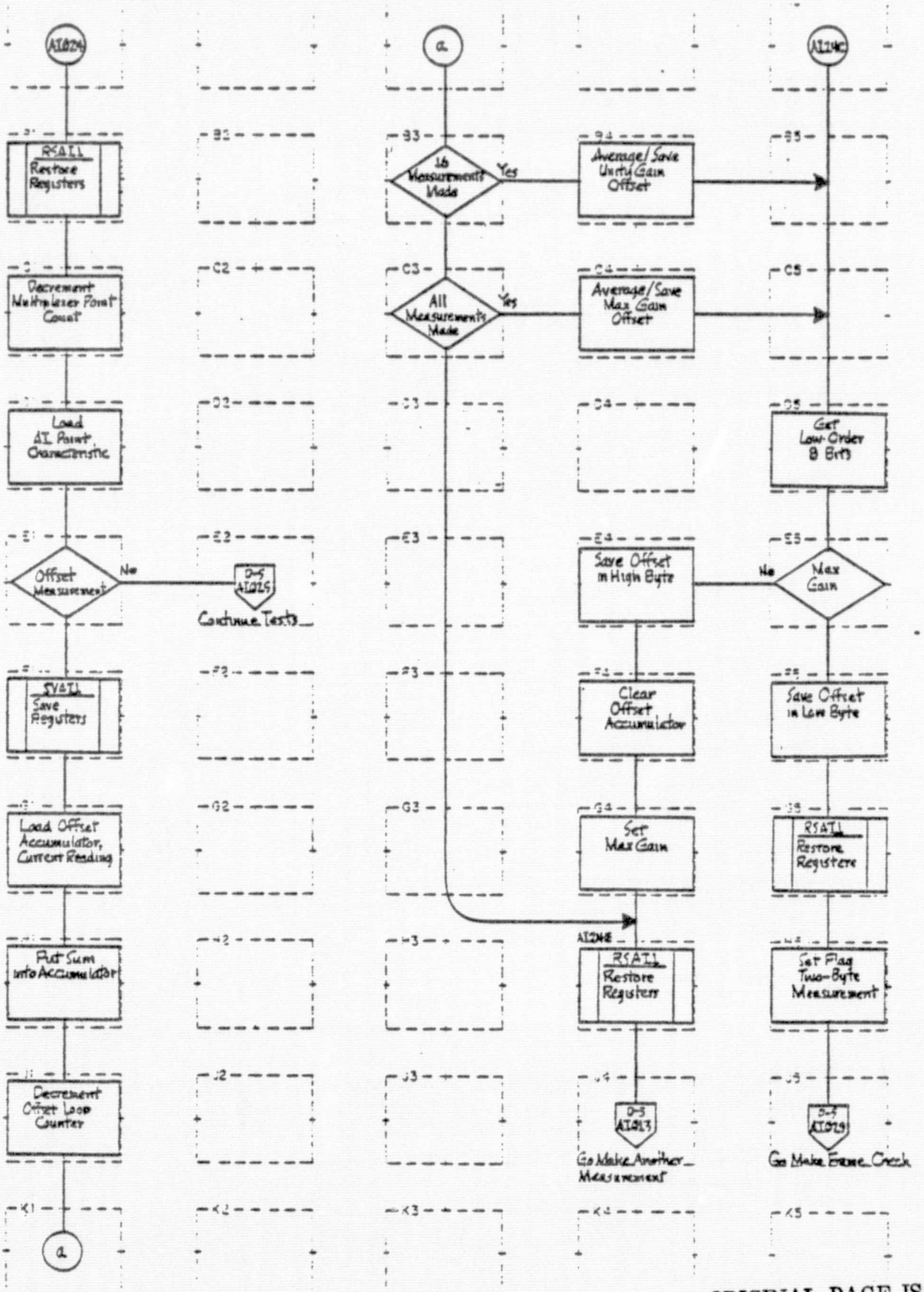

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Figure 8. Analog Input Processing (Page 4 of 6)

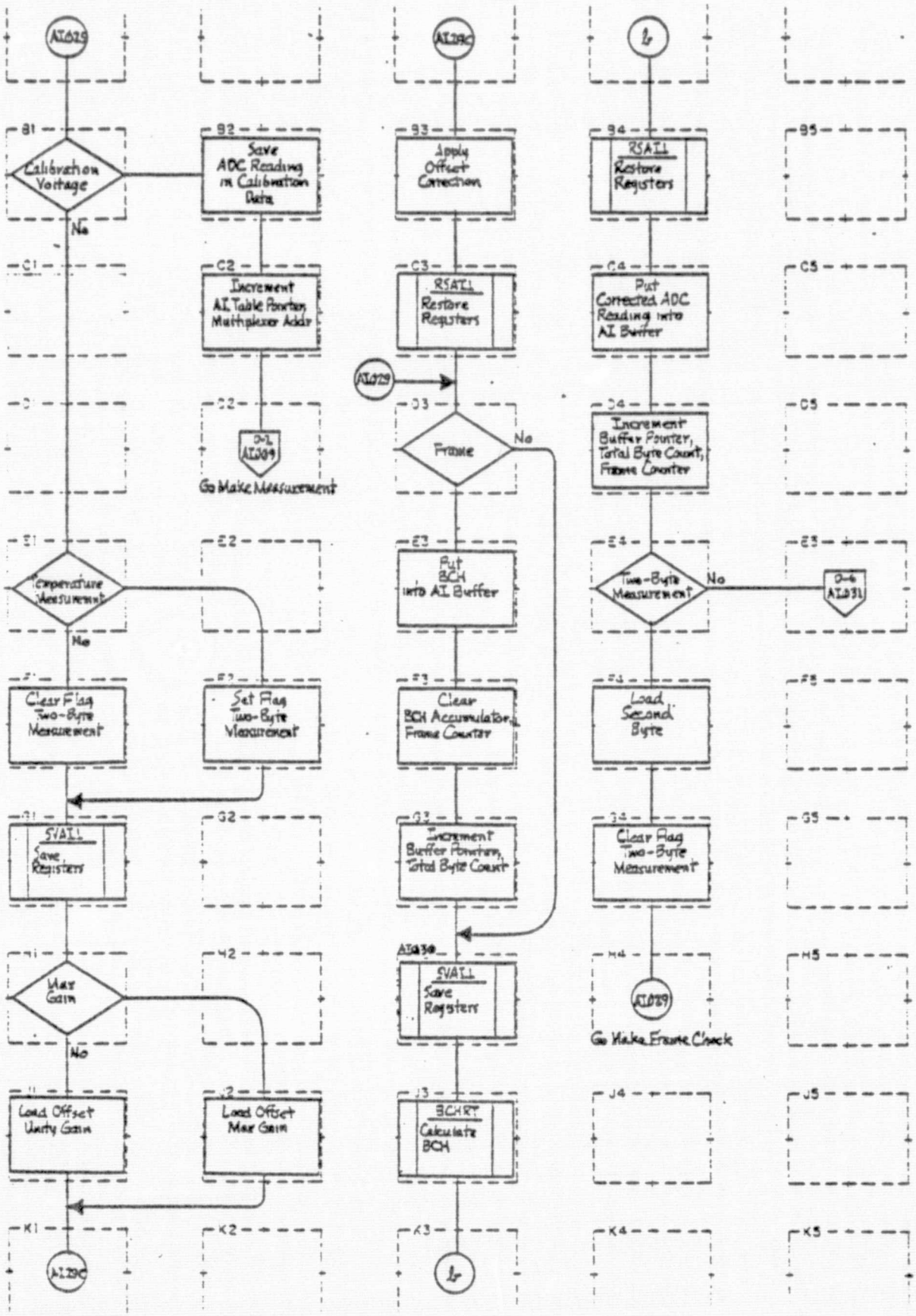

Figure 8. Analog Input Processing (Page 5 of 6)

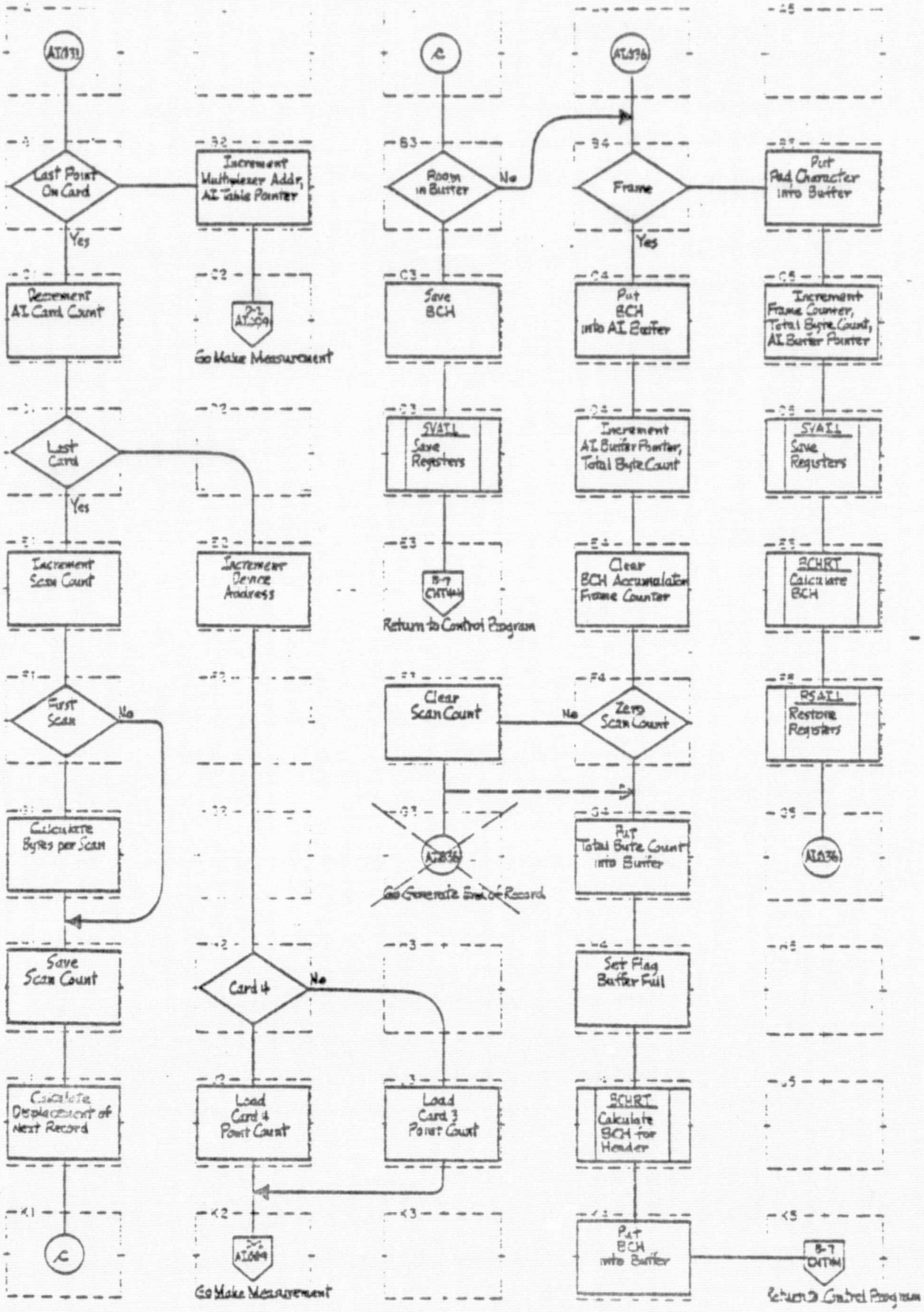

Figure 8. Analog Input Processing (Page 6 of 6)

10. TAPE RECORD (RECRT)

The tape record routine is designed to transfer a variable amount of data from a data buffer to a cassette tape. Either the AI sensor data or an end-of-file flag is placed on the tape.

To execute this routine, interval timer 0 and the tape device must be functioning properly.

INTERVAL TIMERS

Interval timer 0 is used in this routine for 1 second delay to allow the tape recorder to get up to speed before writing any data on the tape.

VARIABLES

TBYCN - maximum byte count

This 2 byte count is set by the AI routine for dumping the buffer or is set to 12 to write the EOF flag.

TBYTE - running byte count

This 2 byte count is updated every time a byte is written to tape. It is used as a compare against TBYCN.

ABORT - A one byte flag, set by the condition code routine, to indicate an error condition. If the ABORT bit is set (to 1) the record routine will (1) branch to the ERROR routine if dumping AI buffer or (2) branch to the communication routine and send error reply if writing EOF flag.

EOTFL - 1 byte flag used to indicate an end-of-file flag is desired. This bit is set by the read configuration and EOF routine.

AI BUFFER DUMP

The AI buffer, BUFFR, is capable of storing 512 bytes of data. This data consists of the read storage table command, sensor readings and BCH characters. The format for the AI buffer is:

PAD/SYNC/COMMAND/STATION ADDRESS/STATUS/RCS/RC2/T1/T2/T3/BCH/8 BYTES OF DATA/BCH/8 BYTES OF DATA/BCH/----/8 BYTES OF DATA/BCH/8 PAD CHARACTERS/BCH

where:

PAD	-	'FF
SYNC	-	'6C'
COMMANDS	-	'EO'
STATION ADDRESS	-	SDAS address (1 byte)
STATUS	-	machine status (1 byte)
RC1 and RC2	-	record count (2 bytes)
T1, T2 and T3	-	time stamp (time communication started - 3 bytes)

END-OF-FILE RECORD

The EOF flag is a 12 byte record which indicates the last record on tape. The format for this marker is:

FF/6C/E1/00/00/00/0B/FF/FF/FF/68/FF

Flow diagram of tape record program is shown in Figure 9.

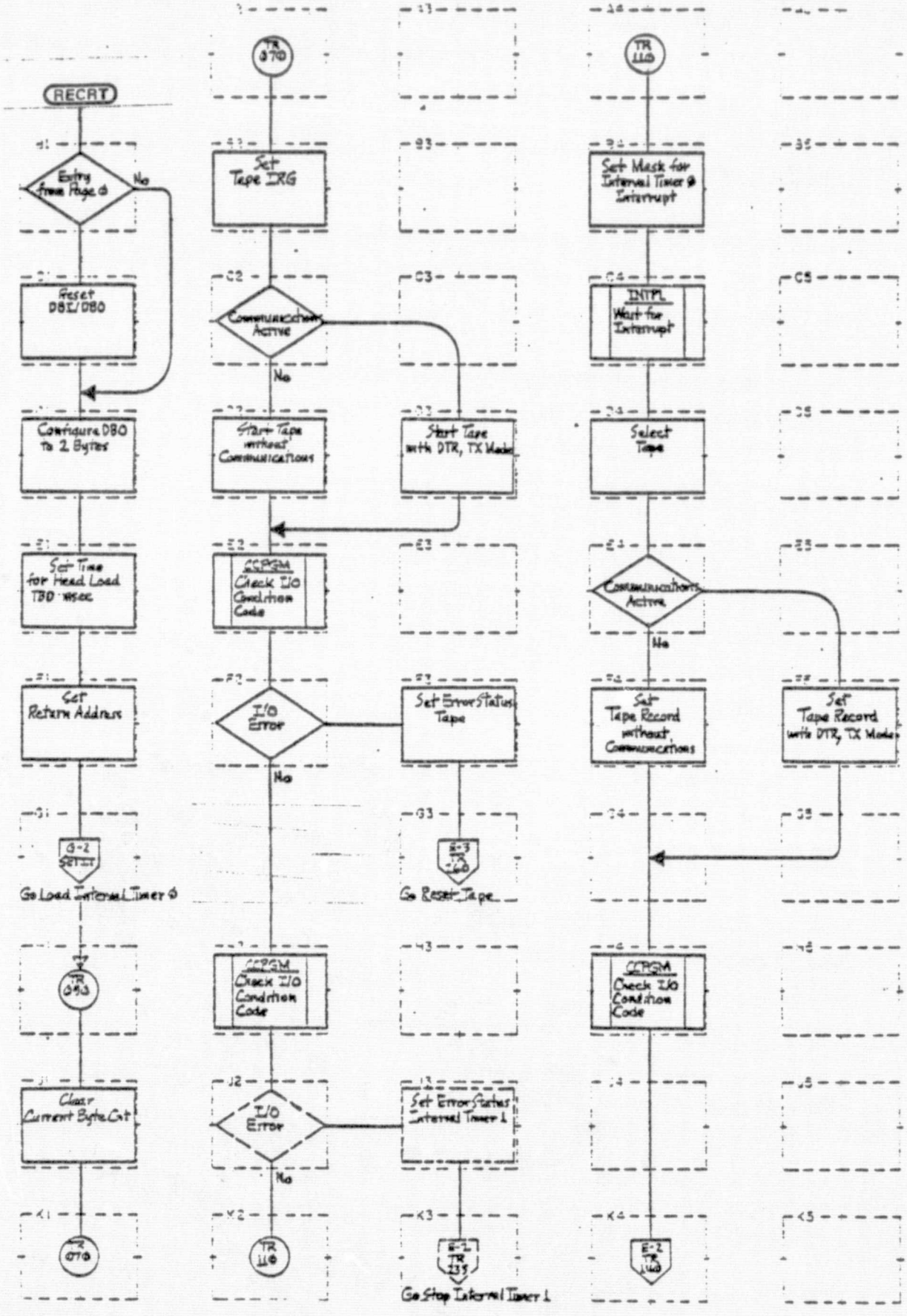

Figure 9. Tape Record Program (Page 1 of 3)

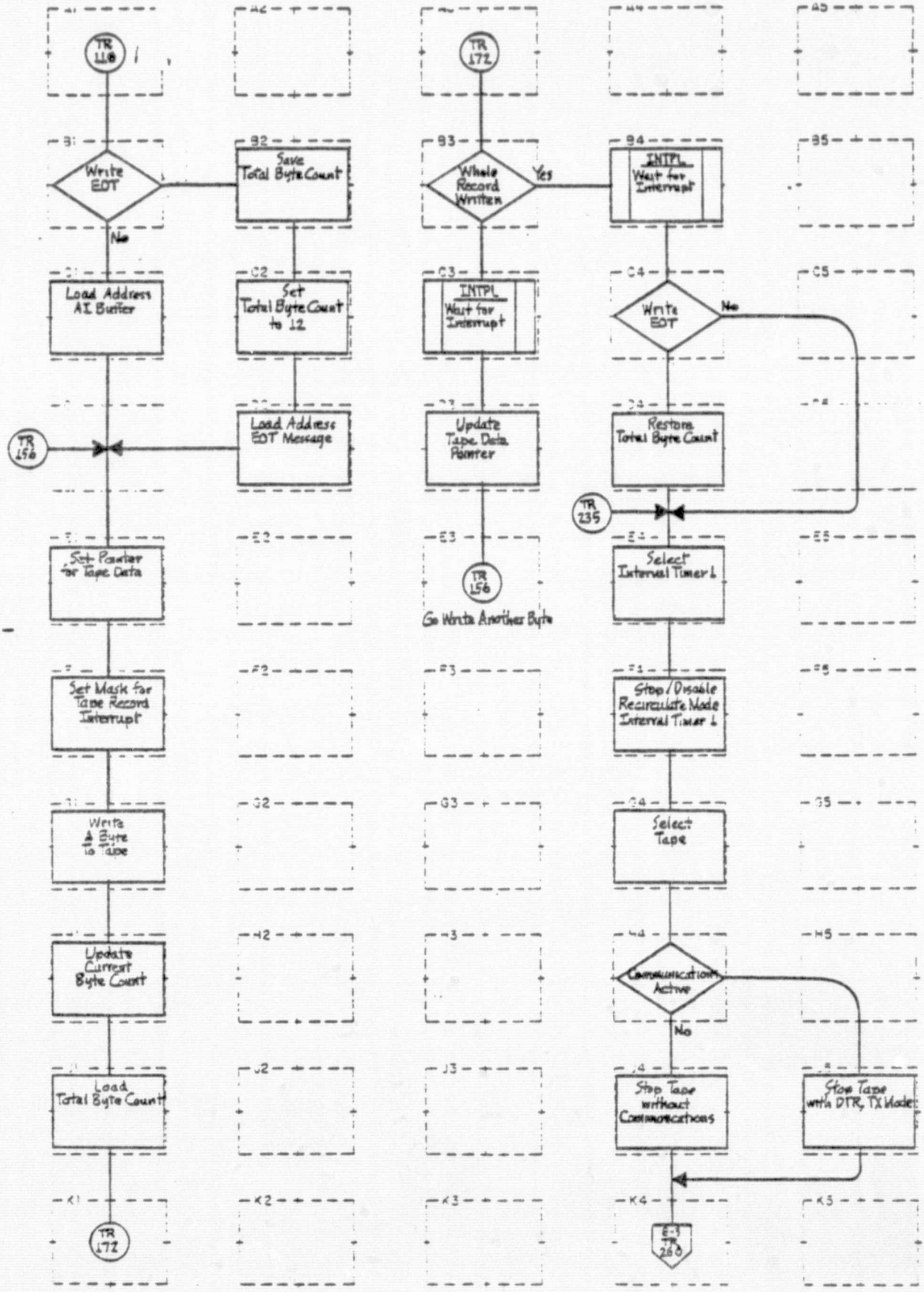

Figure 9. Tape Record Program (Page 2 of 3)

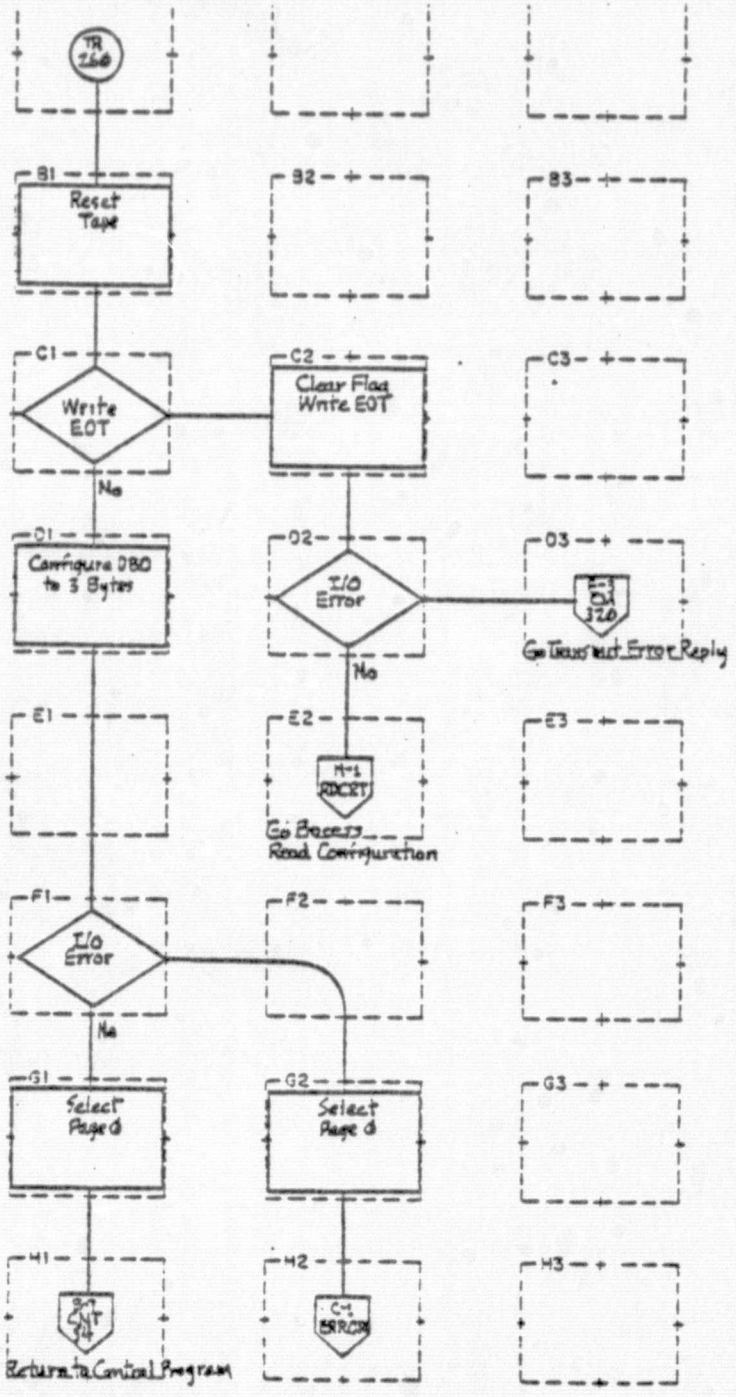

Figure 9. Tape Record Program (Page 3 of 3)

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11. ON-SITE MONITOR/ON-SITE DISPLAY SUPPORT (OSMD)

The On-Site Monitor/On-Site Display Support Program is entered from the interrupt poll program upon occurrence of the OSM/OSD interface interrupt. Upon entry, the program calls the Analog Input Program for reading of sensor inputs. When sensors have been read, the program transfers the data (a byte at the time) to the OSM Microprocessor. The OSMD program generates and transmits an end-of-data word to signal the OSM Microprocessor when data transfer is complete.

SECTION C

PERFORMANCE SPECIFICATION

SITE DATA ACQUISITION SUBSYSTEM (SDAS) MOD 1

DWG NO. 7932905

B

R

REVISIONS

CHK	ENGRG NOTICE	LTR	DESCRIPTION	DATE	APPROVED
	66333ES	-	Original	5/14/76	RED
	66333ZS	A	Revision A (Incorporates Mods M-14, 15, 25, 26, 27)	3/24/77	RED
	66348DC	B	Add "WIND" cmd., microboard type, gas meter, +15V flow meter and minor editing	10/29/77	JES

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TITLE
SITE DATA ACQUISITION SUBSYSTEM
SDAS MOD I PERFORMANCE SPECIFICATION

SIZE	CODE IDENT NO.	DWG NO.
A	20234	7932905

SCALE	WT	SHEET 1 of 24

7932905

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1.0 INTRODUCTION

This specification establishes the requirements for the design and performance of the Model I Site Data Acquisition Subsystem (SDAS). This specification defines the requirements to be met for all configurations of the Site Data Acquisition Subsystem including critical performance, installation requirements, and the detailed configuration relative to the system which it services. The latest revisions to this specification are noted by a heavy line at the right of the modified paragraph.

2.0 APPLICABLE DOCUMENTS

2.1 GOVERNMENT DOCUMENTS

None

2.2 CONTRACTOR DOCUMENTS

7932952 SDAS Mod I Installation Drawing
7933300 SDAS Mod I Acceptance Test Procedure
7932900 32 Channel SDAS I Unit Assembly
7932922 48 Channel SDAS I Unit Assembly

2.3 OTHER DOCUMENTS

None

3.0 GOVERNMENT FURNISHED PROPERTY

None

4.0 SITE DATA ACQUISITION SUBSYSTEM REQUIREMENTS

Requirements for the Site Data Acquisition Subsystem are contained in the following paragraphs.

4.1 SYSTEM OVERVIEW

The Site Data Acquisition Subsystem (SDAS) shall be designed to collect data from sensors located on residential or commercial buildings using a solar heating and/or cooling system. The SDAS shall take the data obtained from sensors located on the solar heating and/or cooling system, process the data into a suitable format, store the data for a period of time, and provide the capability for either telephone retrieval by the Central Data Processing System or manual retrieval of the data for transfer to the central site. The unit shall be designed so it will not degrade the operation of the solar heating/cooling system which it is monitoring.

4.2 OPERATING CHARACTERISTICS

The SDAS provides the flexibility of handling inputs from a maximum of 47 sensors as specified in Paragraph 4.5 for solar energy systems and buildings. Two SDAS configuration options, a 31 channel or a 47 channel option, shall be provided. Individual units shall be personalized for specific site inputs with the personalization options specified in Appendix 1. A functional block diagram of the SDAS is shown in Figure 4.2-1. The SDAS shall perform the following functions:

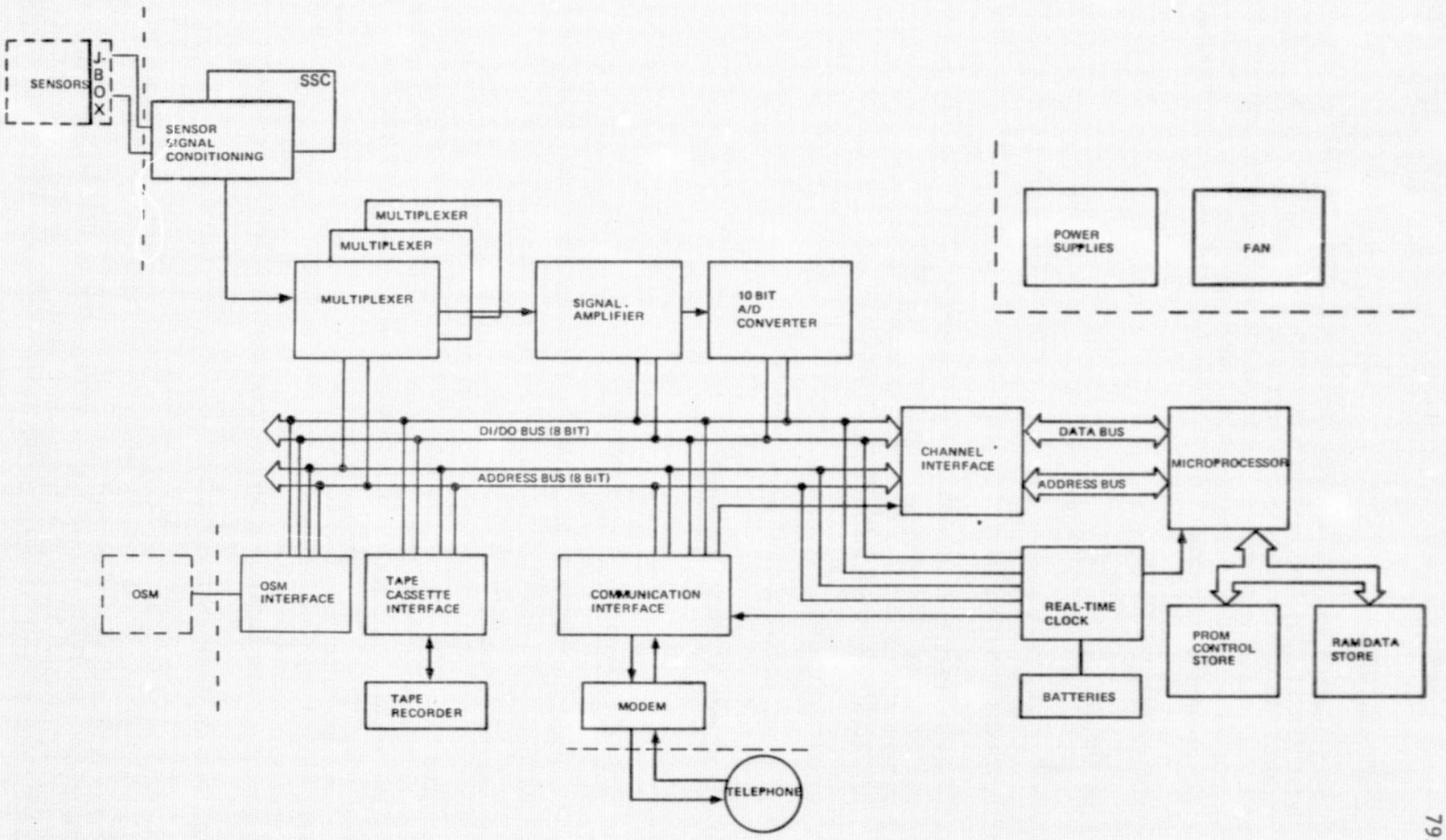

Figure 4.2-1. SDAS Functional Block Diagram

- Scan the input sensors, multiplex, condition and convert the input data into a digital data format.
- Buffer and tape store the data for later retrieval by the central site.
- In response to an interrogation by telephone from the CDPS, transmit the stored data to the CDPS.

The data to be transmitted to the CDPS will be encoded for transmission within the SDAS and transmitted over standard-voice-grade telephone lines. Time, synchronization and BCH (error detecting) codes will be added to the data to aid the CDPS in error detection, formatting and processing of the data from the SDAS.

The CDPS shall have a command/response interface with the SDAS to prevent unauthorized access to the SDAS. The SDAS will provide codes which enable the CDPS to detect the end of the data being transmitted.

4.3 SYSTEM REQUIREMENTS

4.3.1 Time Period

The SDAS shall be designed to operate continuously.

4.3.2. Autonomy

The SDAS shall be designed to operate unattended except for maintenance and manual collection of data.

4.3.3 Subsystem Isolation

The SDAS shall be designed such that a failure of the SDAS shall not affect the operation or performance of the installed solar heating and/or cooling system.

4.3.4 SDAS Safety

Design and installation of the SDAS shall comply with Installation Drawing 7932952 and with applicable codes specified elsewhere in this specification and UL certification requirements to eliminate safety hazards to the occupants of the dwelling or building during SDAS installation and operation.

4.4 PERFORMANCE REQUIREMENTS

4.4.1 Data Scan Interval

A major and a minor scan interval shall be provided. The minor scan interval is 32 seconds and the major scan interval is N x 32 seconds where N=a manually selectable integer from 1 to 127. The baseline major scan interval shall be 320 seconds or 5.33 minutes. Up to 10 asynchronous channels shall be provided in the 48 channel SDAS as specified in Table 4.5-1. These 10 channels will be sampled at the minor scan rate (32 seconds). Other channels shall be sampled at the major scan interval.

The asynchronously scanned channels shall be temporarily stored until each major scan when the average value over the major scan interval will be computed and stored. Approximately 1.5 milliseconds is required to read each sensor input channel.

4.4.2 Analog to Digital Conversion

The SDAS shall convert the analog inputs into 10-bit digital words.

4.4.3 Calibration

A zero volt calibration channel shall be included as an addressable channel (Channel No. 1) for determining the offset accuracy of recorded data.

4.4.4 SDAS Accuracy

The SDAS shall provide a maximum error from multiplexer connector to digital word conversion of the input parameters of 0.4 percent + 1/2 Least Significant Bit of the full scale (5 vdc or 100 mvdc). The sensor signal conditioning in the SDAS shall be included in the sensor error computations.

4.4.5 Time Tag and Coding

The SDAS shall provide a synchronization code and time tags to aid in central site processing. The real-time clock shall operate continuously and shall provide relative time in seconds (2 second resolution) which will be appended to each data scan. The time will be relative (not equal) to real time kept by the CDPS. The clock shall continue to operate during primary power interruptions.

4.4.6 Storage

The SDAS shall provide the capability for tape storage of 1.68 million bits (210 K bytes $\pm$ 10%) of data. The Random Access Memory (RAM) (used for temporary data storage and control program working space) shall have a storage capability of 1K bytes and the control program storage shall have a storage capability of 6K bytes.

4.4.7 Power Supply

The SDAS shall generate the dc voltages required by the SDAS from the 110 vac primary power input. The dc voltages shall be generated by dc power supplies and/or voltage regulators in the SDAS.

4.4.8 Data Retrieval

The collected data can either be manually retrieved by physical removal of the tape casette storage medium or remotely retrieved via a standard voice-grade telephone line interface with the central site.

4.4.9 Data Rate and Format

The data stream shall be formatted for asynchronous transmission over the standard voice-grade telephone lines. The maximum data transmission rate shall be 1.2 KBPS. The CDPS command message, SDAS reply message, SDAS data buffer (RAM Storage), SDAS tape and data transmission formats shall be provided as shown in Figure 4.4-1.

4.4.10 Scan Suspension

The SDAS shall not be required to collect data from the sensors while data is being transmitted to the CDPS site. Scans will also be suspended between writing the "End-of-File" command and the receipt of the "Disconnect" command from the CDPS.

4.4.11 Error Detection

The SDAS shall suspend the collection and processing of sensor inputs when an internal malfunction is detected by the SDAS and shall indicate this suspension when interrogated by the CDPS (SDAS status codes included in reply messages).

4.4.12 CDPS/SDAS Interface

The SDAS shall be capable of receiving and processing the CDPS commands, performing the actions, and transmitting the reply information specified in Table 4.4-1. The data formats and information contained in the CDPS to SDAS command and reply messages shall be as shown in Figure 4.4-1.

4.4.12.1 SDAS Reply Messages

The reply frame of each SDAS reply message (Figure 4.4-1), except the Read Tape and Read Configuration command replies shall include the following items:

- o Command received
- o SDAS station address
- o SDAS status

The "Read Configuration" and "Read Configuration and End-of-File" replies shall additionally include the real-time-clock reading. For a normal reply message, bit 0 of the SDAS status code shall contain a "0" and for an error reply message, bit 0 of the SDAS status code shall contain a "1".

The "Read Tape" reply shall be included on the tape as shown for the buffer format in Figure 4.4-1.

4.4.13 SDAS/OSM Interface

The SDAS shall be capable of accepting an interrupt from the OSM requesting data. In response to the request, the SDAS shall collect data from all input sensors being monitored, shall convert the data to a digital format, and shall transmit the digital data to the OSM. The SDAS shall then resume normal operations. OSM data requests shall be secondary to collection of SDAS normal scans and the OSM request shall not be executed until the SDAS scan is completed.

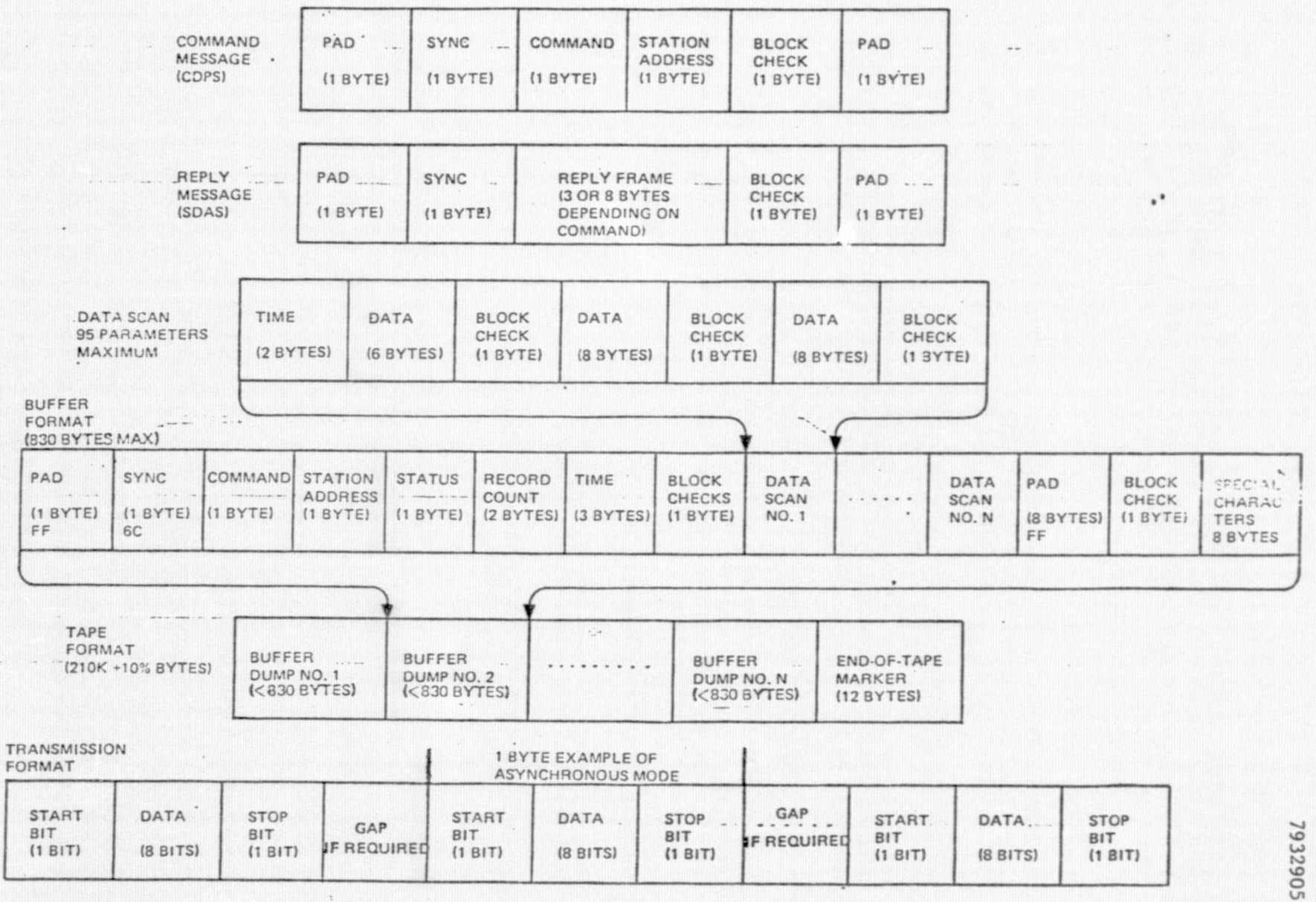

Figure 4.4-1. SDAS Data Formats

Table 4.4-1. CDPS Command and SDAS Reply Requirements

CDPS COMMAND	SDAS ACTION	SDAS REPLY
Read Configuration and End-of-File 'EF'	End of file written to tape cassette	Reply message with current Real-Time-Clock reading sent to CDPS
Rewind 'AA	Tape cassette is rewound and stops on beginning-of-tape (BOT) marker	Reply message sent to CDPS
Read Tape 'E0'	Tape cassette is placed in play back mode	Data on cassette sent as reply message
Disconnect '55'	SDAS disconnected from communications	Reply message sent to CDPS
Disconnect and Rewind '00'	SDAS disconnected from communications and tape cassette rewound	Reply message sent to CDPS
Read Configuration* '2F'	Information gathered for reply message	Reply message sent to CDPS with current SDAS Real-Time-Clock reading
Reinitialize** '1F'	A master reset of SDAS hardware and software executed	Reply message sent to CDPS
Wind '77'	Tape cassette is rewound Past end-of-tape (EOT) marker and stops	Reply message sent to CDPS

* This command useful for verifying status of SDAS
**.Not used during operational data collection

4.5 SDAS INTERFACES

4.5.1 Interface Description

The SDAS shall provide interfaces for connection to the sensors, power, and telephone lines, and On-Site Monitor.

4.5.2 SDAS Primary Power

Power to the SDAS shall be standard 110-125 V, 60 Hertz, 1 Phase, 3 amps service. A 3 wire power cord (safety ground, power and return) shall be required.

4.5.3 Telephone

The SDAS shall interface with a standard Bell System CBS Data Access Arrangement Series 5 or later, or equivalent.

4.5.4 Sensor Interface

The SDAS shall provide the capability to accept data from a maximum of 47 sensors and to interface with the sensors and associated pluggable microboards specified in Appendix 1.

4.5.4.1 Pluggable Microboard Interface

The signal conditioning card(s) included in the SDAS shall provide the capability to accept the pluggable signal conditioning microboards described in Appendix 1. Specific voltage range and signal gain assignment for each input channel is given in Table 4.5-1. The SDAS shall be tested with straight-through wiring on all input channels. The SDAS shall accept inputs in either the 0-5 vdc or 0-100 mvdc range during testing.

4.5.4.2 Sensor Power Requirements

The SDAS shall provide a limited amount of power for use by the attached sensors. Each installed signal conditioning card shall be capable of supplying the following power for use by sensors attached to that card:

3.0 watts at +15 vdc	(200 ma)
0.036 watts at +3.6 vdc	(10 ma)
1.25 watts at +5 vdc	(250 ma)

These levels are the maximum capability of the card. Power utilized by the sensor signal conditioning microboards shall be considered as power supplied to the sensor and must be accounted for in computing the total power required by the sensor.

4.5.5 On-Site Monitor Interface

The On-Site Monitor can be attached to the SDAS through an interface cable which permits the OSM to request and receive an independent scan of measurement data and time from the SDAS.

4.5.6 Detailed SDAS Physical Interfaces

The SDAS shall provide up to six 37-pin connectors for connection with the sensors, the telephone, and OSM interfaces. A standard twist-lock, 3 wire electrical power

connector shall provide for primary power interface. The SDAS I/O connectors pin function assignments for sensor inputs and power outputs are given in Table 4.5-1, and the SDAS/OSM connector pin function assignments are given in Table 4.5-2.

4.6 PACKAGING

4.6.1 Design Environment

The SDAS shall be designed to operate in an indoor environment having temperature extremes between 32°F and 100°F and relative humidity limits of 5% to 80% without condensation.

4.6.2 Modularity

The SDAS shall be designed using modular elements.

4.6.3 Mounting

The SDAS shall be capable of being mounted in accordance with installation drawing 7932952.

4.6.4 Physical Characteristics

The SDAS size shall be approximately 25.5" long x 12" wide x 12" deep and weighs less than 70 pounds.

Add 1" to length to include the case mounted part of I/O connectors, 1.63" to width to include the fan cage and 2" to depth to include mounting ears.

4.7 DESIGN AND CONSTRUCTION

4.7.1 Wiring

All subsystem wiring shall be in compliance with the applicable National Electric Code in effect April 30, 1976.

4.7.2 Failure Protection

UL-recognized circuit protection devices shall be used to provide fault isolation, wiring protection, and shall protect against short circuit hazards. These devices shall comply with the UL code in effect April 30, 1976.

4.7.3 Grounding

Grounding of all electrical/electronic circuitry shall be in accordance with the applicable National Electric Code in effect April 30, 1976.

4.7.4 Component Selection

The electrical and mechanical design shall utilize commercial grade components.

Table 4.5-1. SDAS I/O Pin Function and Channel Allocation (Sheet 1 of 5)

I/O Conn. No.	Sensor Channel or Function	No. I/O Wires	I/O Pin Numbers Hi	Lo	3rd	Input Voltage Acceptable	SDAS Amp Gain	Data Bits Stored	Mux No.	S/C Card No.
J101	1	2	-	-	(Offset Meas. - Internal)				1	1
J101	2(A)	3	3	4	5	0-100 mv	50	10	1	1
J101	3(A)	2	9	10	-	0-100 mv	50	10	1	1
J101	4(A)	3	7	8	6	0-100 mv	50	10	1	1
J101	5(A)	2	13	14	-	0-100 mv	50	10	1	1
J101	6(A)	3	15	16	17	0-100 mv	50	10	1	1
J101	7(A)	2	21	22	-	0-100 mv	50	10	1	1
J101	8(A)	3	19	20	18	0-100 mv	50	10	1	1
J101	9	2	25	26	-	0-100 mv	50	10	1	1
J101	10	3	27	28	29	0-100 mv	50	10	1	1
J101	+5 vdc	1	11						-	1
J101	+3.6 vdc	1	32						-	1
J101	+15 vdc	1	30						-	1
J101	Ground	1	12						-	1
J101	Shield	1	37	-	-				-	-
J101	Spare	9	1-2, 23-24, 31, 33-36						-	-

(A) = Asyncronous Channel (sampled every 32 seconds)

Table 4.5-1. SDAS I/O Pin Function and Channel Allocation (Sheet 2 of 5)

I/O Conn. No.	Sensor Channel or Function	No. I/O Wires	I/O Pin Numbers Hi	Lo	3rd	Input Voltage Acceptable	SDAS Amp Gain	Data Bits Stored	Mux No.	S/C Card No.
J102	11	2	1	2	-	0-100 mv	50	10	1	1
J102	12	3	3	4	5	0-100 mv	50	10	1	1
J102	13	2	9	10	-	0-100 mv	50	10	1	1
J102	14	3	7	8	6	0-100 mv	50	10	1	1
J102	15	2	13	14	-	0-5 v	1	10	1	1
J102	16	3	15	16	17	0-100 mv	50	10	1	1
J102	17	2	21	22	-	0-100 mv	50	10	2	1
J102	18	3	19	20	18	0-100 mv	50	10	2	1
J102	19	2	25	26	-	0-100 mv	50	10	2	1
J102	20	3	27	28	29	0-100 mv	50	10	2	1
J102	21	2	31	32	-	0-100 mv	50	10	2	1
J102	22	3	33	34	30	0-100 mv	50	10	2	1
J102	+3.6 vdc	1	23						-	1
J102	+15 vdc	1	24						-	1
J102	+5 vdc	1	11						-	1
J102	Ground	1	12						-	1
J102	Shield	1	37	-	-				-	-
J102	Spare	2	35	36	-				-	-

Table 4.5-1. SDAS I/O Pin Function and Channel Allocation (Sheet 3 of 5)

I/O Conn. No.	Sensor Channel or Function	No. I/O Wires	I/O Pin Numbers Hi	Lo	3rd	Input Voltage Acceptable	SDAS Amp Gain	Data Bits Stored	Mux No.	S/C Card No.
J103	23	2	1	2	-	0-100 mv	50	10	2	1
J103	24	3	3	4	5	0-100 mv	50	10	2	1
J103	25	2	9	10	-	0-100 mv	50	10	2	1
J103	26	3	7	8	6	0-100 mv	50	10	2	1
J103	27	2	13	14	-	0-100 mv	50	10	2	1
J103	28	3	15	16	17	0-100 mv	50	10	2	1
J103	29	2	21	22	-	0-100 mv	50	10	2	1
J103	30	3	19	20	18	0-100 mv	50	10	2	1
J103	31	2	25	26	-	0-5 v	1	10	2	1
J103	32	3	27	28	29	0-100 mv	50	10	2	1
J103	+5 vdc	1	11						-	1
J103	+3.6 vdc	1	32						-	1
J103	+15 vdc	1	30						-	1
J103	Ground	2	12	31					-	1
J103	Shield	1	37						-	-
J103	Spare	6	23-24, 33-36						-	-

Table 4.5-1. SDAS I/O Pin Function and Channel Allocation (Sheet 4 of 5)

I/O Conn. No.	Sensor Channel or Function	No. I/O Wires	I/O Pin Numbers Hi	Lo	3rd	Input Voltage Acceptable	SDAS Amp Gain	Data Bits Stored	Mux No.	S/C Card No.
J104	33(A)	2	1	2	-	0-100 mv	50	10	3	2
J104	34(A)	3	3	4	5	0-100 mv	50	10	3	2
J104	35(A)	2	9	10	-	0-100 mv	50	10	3	2
J104	36	3	7	8	6	0-100 mv	50	10	3	2
J104	37	2	13	14	-	0-100 mv	50	10	3	2
J104	38	3	15	16	17	0-100 mv	50	10	3	2
J104	39	2	21	22	-	0-100 mv	50	10	3	2
J104	40	3	19	20	18	0-100 mv	50	10	3	2
J104	41	2	25	26	-	0-5 v	1	10	3	2
J104	42	3	27	28	29	0-100 mv	50	10	3	2
J104	+5 vdc	1	11	-	-			-	-	2
J104	+3.6 vdc	1	32	-	-			-	-	2
J104	+15 vdc	1	30	-	-			-	-	2
J104	Ground	1	12		-			-	-	2
J104	Shield	1	37	-	-			-	-	-
J104	Spare	7	23-24	33-36	31			-	-	-

(A) = Asynchronous Channel (sampled every 32 seconds)

Table 4.5-1. SDAS I/O Pin Function and Channel Allocation (Sheet 5 of 5)

I/O Conn. No.	Sensor Channel or Function	No. I/O Wires	I/O Pin Numbers Hi	Lo	3rd	Input Voltage Acceptable	SDAS Amp Gain	Data Bits Stored	Mux No.	S/C Card No.
J105	43	3	1	2	3	0-100 mv	50	10	3	2
J105	44	3	5	6	4	0-100 mv	50	10	3	2
J105	45	3	9	10	11	0-100 mv	50	10	3	2
J105	46	3	13	14	12	0-100 mv	50	10	3	2
J105	47	3	17	18	19	0-100 mv	50	10	3	2
J105	48	3	21	22	20	0-100 mv	50	10	3	2
J105	+5 vdc	1	7	-	-	-	-	-	-	2
J105	+3.6 vdc	1	15	-	-	-	-	-	-	2
J105	+15 vdc	1	23	-	-	-	-	-	-	2
J105	Ground	1	16	-	-	-	-	-	-	2
J105	Shield	1	28	-	-	-	-	-	-	-
J105	Ring Indicator	1	30	-	-	-	-	-	-	-
J105	Data Modem Ready	1	31	-	-	-	-	-	-	-
J105	Switch Hook	1	32	-	-	-	-	-	-	-
J105	Off Hook	1	33	-	-	-	-	-	-	-
J105	Coupler Cut Through	1	34	-	-	-	-	-	-	-
J105	Coupler Ground	1	35	-	-	-	-	-	-	-
J105	Data Ring	1	36	-	-	-	-	-	-	-
J105	Data Tip	1	37	-	-	-	-	-	-	-
J105	Spare	6	24-27	29	8	-	-	-	-	-

Table 4.5-2. SDAS/OSM Interface Connector Pin Function and Channel Allocation

PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
01		18	
02		19	
03		20	
04		21	
05		22	SDAS TO OSM DBO BIT 0
06		23	1
07		24	2
08		25	3
09	-OSM CARD SELECT	26	4
10	-INTERRUPT POLL	27	5
11	-OSM INTERRUPT REQUEST	28	6
12	-OSM SELECT ACKNOWLEDGE	29	7
13	-AI STROBE	30	
14	FUNCTION BIT 0	31	
15	FUNCTION BIT 1	32	-OSM CONNECTED
16		33	SIGNAL RETURN
17		34	
		35	
		36	
		37	

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4.7.5 Fungi/Mildew Resistance

Components of the system shall not support the growth of fungi, mold, and/or mildew in the presence of moisture to an extent that will impair their operational function over their intended service life.

4.7.6 Materials Compatibility

Component materials used in the subsystem shall be selected to minimize corrosion and deterioration that could degrade component performance under operating conditions.

4.7.7 Dissimilar Materials

Dissimilar materials and dissimilar materials coated with corrosion resistant finishes, when used in contact with each other, shall not create corrosive deterioriation which interferes with mechanical or electrical performance of the SDAS or its associated parts.

4.7.8 Interchangeability

Mechanical and electrical interchangeability and replaceability shall exist in form, fit, and function of assemblies and subassemblies of the same part numbers.

4.7.9 Marking

Marking of the SDAS shall be in accordance with good commercial practices in order to facilitiate assembly, checkout and maintenance.

4.7.10 Workmanship

Workmanship in fabrication and assembly of the SDAS shall be consistent with good commercial practices.

4.7.11 Safety

The SDAS shall be UL certified.

4.7.12 Fire Prevention

The SDAS shall conform to the fire section of applicable national fire codes in effect April 30, 1976.

4.8 RELIABILITY/MAINTAINABILITY

4.8.1 Maintenance/Replaceable Units

The SDAS shall be of a modular design to permit replacement of failed subassemblies.

4.8.2 Accessibility

The SDAS shall be designed to assure that field replaceable items shall be accessible for servicing, removal, or replacement.

4.8.3 Reliability

The SDAS shall use commercial grade components and shall be designed not to adversely affect the operation and performance of the monitored system.

4.8.4 Serviceability

The SDAS shall be capable of being serviced with a minimum amount of special equipment by a trained field technician.

5.0 GEOGRAPHICAL AREA

The SDAS shall be capable of operating in any geographic area of the United States subject to the restrictions specified elsewhere in this specification.

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APPENDICES

APPENDIX 1

SDAS SITE PERSONALIZATION

1.0 INTRODUCTION

This appendix defines the SDAS design options which may be used to personalize the SDAS to meet site unique requirements which do not conform with the requirements stated in the main body of this specification.

This appendix defines the options which could be implemented into the unit assembly during personalization, into the microcode during SDAS Programmable Read Only Memory (PROM) burn-in, and defines for each sensor the microboard circuits which plug into the SDAS signal conditioning card and which are used to condition the sensor inputs to interface with the SDAS multiplexer card(s).

2.0 PROM MICROCODE OPTIONS

A standard predefined microcode PROM program is used in the SDAS for as many sites as possible. Table 4.5-1 gives the standard amplifier gain, data bits stored and asynchronous channel assignments for the standard PROM. To meet some site unique requirements, a site unique microcode program may be made for that site. The standard microcode program may be altered by assigning an amplifier gain of 1 or 50 and/or the number of data bits stored equal to 8 or 10 for each sensor channel. As an additional option, the ten asynchronous channels may be assigned to any of the sensor channels. No other options are available for the present microcode design.

3.0 SENSOR INTERFACE AND SIGNAL CONDITIONING MICROBOARDS

Table 3-1 lists the sensors which provide inputs to the SDAS, the sensor interface characteristics, and the microboards required to interface these sensors with the SDAS.

Four standard types of signal conditioning circuits shall be mounted on pluggable microboards which plug into mounting sockets included on the SDAS signal conditioning cards. The microboard types for each acceptable sensor are shown in Table 3-1. The following signal conditioning circuits shall be provided.

3.1 STRAIGHT THROUGH WIRING

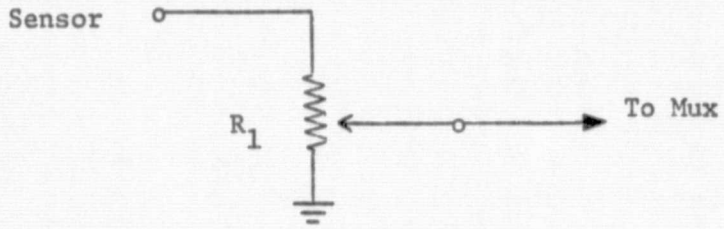
Analog or digital discrete inputs of 0 to 5 vdc or 0 to 100 millivolts dc shall not require conditioning, and microboards wiring the sensor input directly to the multiplexer input shall be provided.

3.2 DIVIDER NETWORK

A pluggable microboard with a divider network shall be provided to condition sensor outputs to 0-5 vdc or 0-100 mvdc as specified in Table 3-1. The divider network shall be as follows:

Table 3-1. Sensor Interface and Microboard Requirements

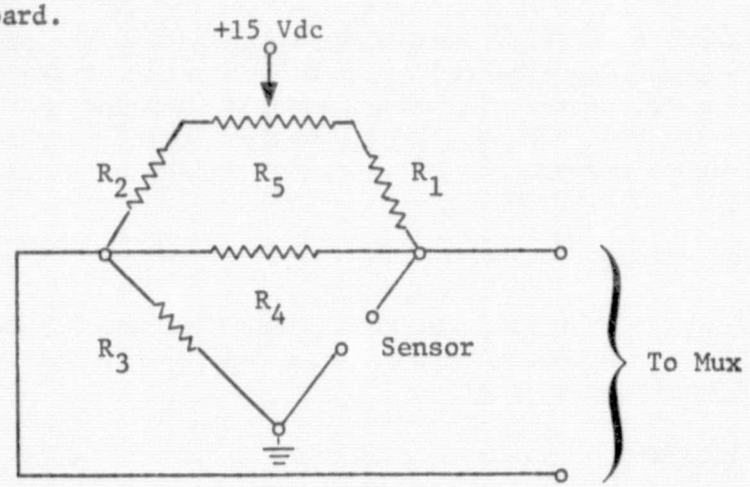
CHANNEL UTILIZATION	SENSOR INPUT	SENSOR OUTPUT	SDAS AMPLIFIER GAIN	NO. WIRES	MICROBOARD TYPE
Pyranometer	---	0-12 mvdc	50	2 + S	Straight Through
Resistance Thermal Detector (RTD)	+15 vdc 15 ma	0-100 mvdc	50	2/3 + S	Temperature Bridge
Delta RTD	+15 vdc 20 ma	0-100 mvdc	50	3 + S	Delta Temperature Bridge
Target Type Flowmeter	+5.0 vdc 15 ma	0-10 mvdc	50	4 + S	Straight Through
Target Type Flowmeter	+15.0 vdc 45 ma	0-30 mvdc	50	4 + S	Straight Through
Hot Wire Anonometer (Air Flow)	115 vac	0-5 vdc	1	2 + S	Straight Through or Voltage Divider
Gas Meter	+5 vdc	0-5 vdc	1	3 + S	Straight Through
Wattmeter	---	0-50 mvdc 0-100 mvdc 0-150 mvdc	50	2 + S	Straight Through or Voltage Divider
Humidity	+3.6 vdc 10 ma	0-100 mvdc	50	4 + S	Straight Through
Wind Speed	---	13.3 vdc @ 100 mph	1	2 + S	Voltage Divider
Wind Direction	+5 vdc 10 ma	0-5 vdc	1	3 + S	Straight Through or Voltage Divider
Unused Channels	---	---	--	---	Input Shorting



NOTE: The specific voltage values are dependent upon the range of the input and output voltages and shall be selected to maximize output values. Currently R_1 is a potentiometer which is manually set to the required divider network ratio.

3.3 TEMPERATURE BRIDGE

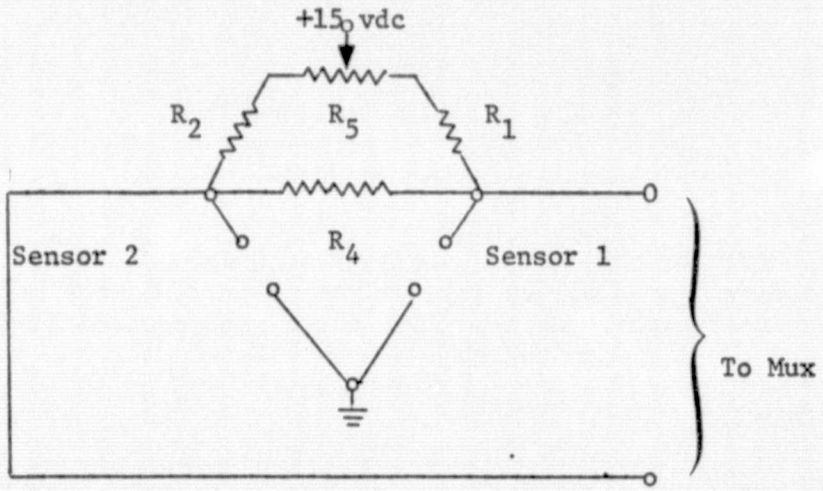
Analog inputs from a 100 ohm resistance thermal detector shall be conditioned to a 0 to 100 mvdc output using the following circuit; and the circuit shall be mounted on a pluggable microboard.



NOTE: The specific resistor values are dependent on the range of the input temperature being measured and shall be selected to meet performance evaluation accuracy requirements. Temperature range values selected for implementation include 30°F to 230°F, 30°F to 160°F, 30°F to 450°F, and -20°F to 120°F.

3.4 DELTA TEMPERATURE BRIDGE

Analog inputs from 100 ohm resistance thermal detectors used to measure differential temperatures shall be conditioned to a 0 to 100 mvdc output using the following circuit and the circuit shall be mounted on a pluggable microboard.



NOTE: The specific resistor values are dependent on the range of the input delta temperature being measured and the base value of the temperature from which the delta temperature is being measured, and shall be selected to meet performance evaluation accuracy requirements. Delta temperature range values and base for delta temperature selected for implementation include 0°F to 50°F, 0°F to 100°F, and 0°F to 80°F.

3.5 INPUT SHORTING NETWORK

A pluggable microboard with wiring which ties the high and low input signals together shall be provided for input channels which are read by the microprocessor, but which have no sensor input on the channel.

3.6 TERMINATING RESISTOR

A pluggable microboard with a terminating resistor shall be used to convert a current input source to a voltage output.

SECTION D

DESIGN DRAWINGS LIST

The attached list of drawings reflect the design of the Site Data Acquisition Subsystem as designed and built by the International Business Machines Corporation. These drawings are restricted to quotation or build.

Dwg #	Title
CC030	Comm Card Controls & Condition Code Logic
CC042	Command & Address Decode
CC050	Status & ID Control Logic
CC060	Tape & Comm Control and Status Reg.
CC070	Comm. Logic (UART)
CC080	UART Control Logic
CC100	Output Buffers (Cond. Code and Card I. D.)
CC101	Output Buffers (Tape & Comm Status)
CN001	Comm Card to Kite Channel Interface Entry/Exit
CN002	Comm Card to Modem Entry/Exit
CN003	Comm Card to Tape Entry/Exit
CN010	Input Buffers Kite Interface
TC015	Tape Interface Serdes & Interrupts
TC016	Tape Logic Receivers
TC017	Tape Control Logic I
TC018	Tape Control Logic II
TC019	Tape Control Logic III
7932851	Back Panel Asm
7932860	Multiplexer w/Amp, Card
7932861	Solid State Mpxr + Amp Asm
7932864	Schematic Solid State Multiplexer + Amplifier
7932870	Multiplexer without Amp, Card
7932871	Solid State Multiplexer
7932872	Gasket, Lower Terminals
7932873	Gasket, Upper Terminals
7932874	Schematic, Solid State Multiplexer
7932875	Solid State Multiplexer
7932880	AI Basic, Card
7932881	AI Basic Card, ASM
7932884	Schematic AI Basic
7932897	Holder, Card Three High-Four Wide
7932900	SDCS Unit Assy
7932910	Detail, Interface Card
7932911	Interface Card Asm
7932922	SDCS Unit Assy
7932923	Clip, Page Holding
7932926	Gasket, Wrap
7932930	Regulator Card
7932931	Regulator Card Asm
7932933	Insulator
7932935	Insulator
7932937	Holder - Card Six High CBM

Dwg #	Title
7932939	Microboard Asm
7932942	Plate, Upper
7932943	Plate, Lower
7932946	Gasket, Lower
7932947	Cable Assembly
7932949	Schematic Electrical, Prom Card
7932952	SDAS Installation Drawing
7932955	Cover, Plenum
7932956	Ramp, Air Flow
7932957	Cover, Fan
7932960	Cable Assembly Interface/Backpanel
7932961	Tape Recorder, Phi Deck Fixed Speed 1-7/8
7932962	Read Write Electronics Asm
7932963	Control Electronics Assembly
7932966	Shield, Safety
7932968	Cable Recorder I/O
7932969	Insulator Regulator
7932970	Printed Wiring Board
7932971	Printed Wiring Board Asm, Pwr Supply
7932973	Bracket, Recorder
7932974	Spacer - Long, Recorder
7932976	Bracket, Component Support
7932979	SDAS Power Tub/Regulator Asm
7932980	Card, Signal Conditioning
7932981	Card, Signal Conditioning Asm
7932983	Schematic, Electrical Card, Signal Conditioning
7932985	Microboard Asm Type I
7932991	Cable Assembly
7932992	Cable Assembly
7932993	Cable Assembly
7933018	Cable Assy Panel SDAS Power Distr.
7933019	Cable Asm, Battery
7933020	Cable Assembly
7933021	Cable Assembly I/O 4
7933022	Cable Assembly I/O 3
7933023	Cable Assembly 2
7933024	Cable Assembly I/O 1
7933026	Cable Asm Fan
7933027	Recorder Assy
7933030	Cable, Recoder Power
7933033	Cover, Assembly

Dwg #	Title
7933034	Frame, SDAS
7933035	Resistor Assembly
7933036	Power Supply Housing
7933040	Spacer, Short
7933041	Support, Guide
7933042	Rail, Backpanel
7933043	Rail, Backpanel
7933044	Bracket, Resistor
7933045	Spacer, Long
7933046	Frame, Panel
7933047	Gasket, Connector
7933048	Plate, Cover Conn.
7933049	Cage Assembly
98M30067	Electrical Schematic Board 4

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